

Virtex-6 Family FPGAs



		Virtex-6 LXT FPGAs Optimized for High-performance Logic and DSP with Low-power Serial Connectivity (1.0 Volt, 0.9 Volt)						Virtex-6 SXT FPGAs Optimized for Ultra High-performance DSP with Low-power Serial Connectivity (1.0 Volt, 0.9 Volt)		Virtex-6 HXT FPGAs Optimized for Communications Systems Requiring Highest-bandwidth Serial Connectivity (1.0 Volt)				
Part Number		XC6VLX75T	XC6VLX130T	XC6VLX195T	XC6VLX240T	XC6VLX365T	XC6VLX550T	XC6VLX760	XC6VVSX315T	XC6VVSX475T	XC6VHX250T	XC6VHX255T	XC6VHX380T	XC6VHX565T
EasyPath™ FPGA Cost Reduction Solutions (1)		XC6VLX75T	XC6VLX130T	XC6VLX195T	XC6VLX240T	XC6VLX365T	XC6VLX550T	XC6VLX760	XC6VVSX315T	XC6VVSX475T	XC6VHX250T	XC6VHX255T	XC6VHX380T	XC6VHX565T
Logic Resources	Slices (2)	11,640	20,000	31,200	37,680	56,880	85,920	118,560	49,200	74,400	39,360	39,600	59,760	88,560
	Logic Cells (3)	74,496	128,000	199,680	241,152	364,032	549,888	758,784	314,880	476,160	251,904	253,440	382,464	566,784
	CLB Flip-Flops	93,120	160,000	249,600	301,440	455,040	687,360	948,480	393,600	595,200	314,880	316,800	478,080	708,480
Memory Resources	Maximum Distributed RAM (Kbits)	1,045	1,740	3,040	3,650	4,130	6,200	8,280	5,090	7,640	3,040	3,050	4,570	6,360
	Block RAM/FIFO w/ ECC (36Kbits each)	156	264	344	416	416	632	720	704	1,064	504	516	768	912
	Total Block RAM (Kbits)	5,616	9,504	12,384	14,976	14,976	22,752	25,920	25,344	38,304	18,144	18,567	27,648	32,832
Clock Resources	Mixed Mode Clock Managers (MMCM)	6	10	10	12	12	18	18	12	18	12	12	18	18
I/O Resources (4, 5)	Maximum Single-Ended I/O	360	600	600	720	720	1,200	1,200	720	840	320	480	720	720
	Maximum Differential I/O Pairs	180	300	300	360	360	600	600	360	420	160	240	360	360
Embedded Hard IP Resources (6)	DSP48E1 Slices	288	480	640	768	576	864	864	1,344	2,016	576	576	864	864
	PCI Express® Interface Blocks	1	2	2	2	2	2	–	2	2	4	2	4	4
	10/100/1000 Ethernet MAC Blocks	4	4	4	4	4	4	–	4	4	4	2	4	4
	GTX Low-Power Transceivers	12	20	20	24	24	36	–	24	36	48	24	48	48
	GTX High-Speed Transceivers	–	–	–	–	–	–	–	–	–	–	24	24	24
Speed Grades	Commercial	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2, -3	-L1, -1, -2	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2
	Industrial	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1	-L1, -1	-L1, -1, -2	-L1, -1	-1, -2	-1, -2	-1, -2	-1
Configuration	Configuration Memory (Mbits)	25.0	41.7	58.7	70.4	91.6	137.4	176.3	99.6	149.4	76.2	76.2	114.2	153.2
Package (7)		Area												
		Available User I/O: SelectIO Pins (8, 9) (GTX Low-power Transceivers, GTX High-speed Transceivers)												
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)														
FF484	23 x 23 mm	240 (8, 0)	240 (8, 0)											
FF784	29 x 29 mm	360 (12, 0)	400 (12, 0)	400 (12, 0)	400 (12, 0)									
FF1156	35 x 35 mm		600 (20, 0)	600 (20, 0)	600 (20, 0)	600 (20, 0)			600 (20, 0)	600 (20, 0)				
FF1759	42.5 x 42.5 mm				720 (24, 0)	720 (24, 0)	840 (36, 0)		720 (24, 0)	840 (36, 0)				
FF1760	42.5 x 42.5 mm						1,200 (0, 0)	1,200 (0, 0)						
FF1154	35 x 35 mm										320 (48, 0)		320 (48, 0)	
FF1155	35 x 35 mm											440 (24, 12)	440 (24, 12)	
FF1923	45 x 45 mm											480 (24, 24)	720 (40, 24)	720 (40, 24)
FF1924	45 x 45 mm												640 (48, 24)	640 (48, 24)

- Notes:
1. EasyPath™ solutions provide a conversion-free, low-risk path for volume production.
 2. A single Virtex-6 FPGA CLB comprises two slices, with each containing four 6-input LUTs and eight Flip-Flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-LUTs and 16 Flip-Flops per CLB.
 3. Virtex-6 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
 4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
 5. I/O standards supported: HT, LVCMOS (2.5V, 1.8V, 1.5V, 1.2V), HSTL I (1.2V, 1.5V, 1.8V), HSTL II (1.5V, 1.8V), HSTL III (1.5V, 1.8V), LVDS, Extended LVDS, RSDS, Bus LVDS, LVPECL, SSTL I (1.8V, 2.5V), SSTL II (1.8V, 2.5V), SSTL (1.5V).
 6. One system monitor block included in all devices.
 7. All products available Pb-free and RoHS-Compliant (FFG).
 8. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com/virtex6

Virtex-5 Family FPGAs



		Virtex®-5 LX FPGAs Optimized for High-performance Logic (1.0 Volt)						Virtex-5 LXT FPGAs Optimized for High-performance Logic with Low-power Serial Connectivity (1.0 Volt)								
Part Number		XC5VLX30	XC5VLX50	XC5VLX85	XC5VLX110	XC5VLX155	XC5VLX220	XC5VLX330	XC5VLX20T	XC5VLX30T	XC5VLX50T	XC5VLX85T	XC5VLX110T	XC5VLX155T	XC5VLX220T	XC5VLX330T
EasyPath™ Cost Reduction Solutions (1)		—	—	XC5VLX85	XC5VLX110	XC5VLX155	XC5VLX220	XC5VLX330	—	—	—	XCEVLX85T	XC5VLX110T	XC5VLX155T	XC5VLX220T	XC5VLX330T
Logic Resources	Slices (2)	4,800	7,200	12,960	17,280	24,320	34,560	51,840	3,120	4,800	7,200	12,960	17,280	24,320	34,560	51,840
	Logic Cells (3)	30,720	46,080	82,944	110,592	155,648	221,184	331,776	19,968	30,720	46,080	82,944	110,592	155,648	221,184	331,776
	CLB Flip-Flops	19,200	28,800	51,840	69,120	97,280	138,240	207,360	12,480	19,200	28,800	51,840	69,120	97,280	138,240	207,360
	Maximum Distributed RAM (Kbits)	320	480	840	1,120	1,640	2,280	3,420	210	320	480	840	1,120	1,640	2,280	3,420
Memory Resources	Block RAM/FIFO w/ECC (36Kbits each)	32	48	96	128	192	192	288	26	36	60	108	148	212	212	324
	Total Block RAM (Kbits)	1,152	1,728	3,456	4,608	6,912	6,912	10,368	936	1,296	2,160	3,888	5,328	7,632	7,632	11,664
	Digital Clock Managers (DCM)	4	12	12	12	12	12	12	2	4	12	12	12	12	12	12
Clock Resources	Phase Locked Loop (PLL)/PMCD	2	6	6	6	6	6	6	1	2	6	6	6	6	6	6
	Maximum Single-Ended Pins	400	560	560	800	800	800	1,200	172	360	480	480	680	680	680	960
I/O Resources (4,5)	Maximum Differential I/O Pairs	200	280	280	400	400	400	600	86	180	240	240	340	340	340	480
	I/O Standards	HT, LVDS, LVDSxT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II														
Embedded (6) Hard IP Resources	DSP48E Slices	32	48	48	64	128	128	192	24	32	48	48	64	128	128	192
	PowerPC® 440 Processor Blocks	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	PCI Express® Endpoint Blocks	—	—	—	—	—	—	—	1	1	1	1	1	1	1	1
	10/100/1000 Ethernet MAC Blocks	—	—	—	—	—	—	—	2	4	4	4	4	4	4	4
	RocketIO™ GTP Low-Power Transceivers	—	—	—	—	—	—	—	4	8	12	12	16	16	16	24
	RocketIO™ GTX High-Speed Transceivers	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Speed Grades	Commercial	-1,-2,-3	-1,-2,-3	-1,-2,-3	-1,-2,-3	-1,-2,-3	-1,-2	-1,-2	-1,-2	-1,-2,-3	-1,-2,-3	-1,-2,-3	-1,-2,-3	-1,-2,-3	-1,-2	-1,-2
	Industrial	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1
Configuration	Configuration Memory (Mbits)	8.4	12.6	21.9	29.1	41.1	53.2	79.8	6.3	9.4	14.1	23.4	31.2	43.1	55.2	82.7
Package (7)		Area Available User I/O: Select I/O Interface Pins (GTP/GTX Serial Transceivers)														
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)																
	FF324	19 x 19 mm	220	220												
	FF676	27 x 27 mm	400	440	440	440										
	FF1153	35 x 35 mm		560	560	800	800									
	FF1760	42.5 x 42.5 mm				800	800	800	1200							
	FF323	19 x 19 mm								172 (4)	172 (4)					
	FF665	27 x 27 mm									360 (8)	360 (8)				
	FF1136	35 x 35 mm										480 (12)	480 (12)	640 (16)	640 (16)	
	FF1738	42.5 x 42.5 mm												680 (16)	680 (16)	680 (16) 960 (24)
	FF1156	35 x 35 mm														
	FF1759	42.5 x 42.5 mm														

- Notes:
- EasyPath™ solutions provide a conversion-free and low risk path for volume production.
 - A single Virtex-5 FPGA comprises two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
 - Virtex-5 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
 - Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
 - I/O standards supported HT, LVDS, LVDSxT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II
 - One system monitor block included in all devices.
 - All products available Pb-free and RoHS-Compliant.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com/virtex5

Virtex-5 Family FPGAs



		Virtex-5 SXT FPGAs Optimized for DSP with Low-power Serial Connectivity (1.0 Volt)				Virtex-5 FXT FPGAs Optimized for Embedded Processing with High-Speed Serial Connectivity (1.0 Volt)					Virtex-5 TXT FPGAs Optimized for Ultra-High Bandwidth (1.0 Volt)	
Part Number		XC5VSX35T	XC5VSX50T	XC5VSX95T	XC5VSX240T	XC5VFX30T	XC5VFX70T	XC5VFX100T	XC5VFX130T	XC5VFX200T	XC5VTX150T	XC5VTX240T
EasyPath™ Cost Reduction Solutions (1)		—	XC5VSX50T	XC5VSX95T	XC5VSX240T	—	XC5VFX70T	XC5VFX100T	XC5VFX130T	XC5VFX200T	XC5VTX150T	XC5VTX240T
Logic Resources	Slices (2)	5,440	8,160	14,720	37,440	5,120	11,200	16,000	20,480	30,720	23,200	37,440
	Logic Cells (3)	34,816	52,224	94,208	239,616	32,768	71,680	102,400	131,072	196,608	148,480	239,616
	CLB Flip-Flops	21,760	32,640	58,880	149,760	20,480	44,800	64,000	81,920	122,880	92,800	149,760
Memory Resources	Maximum Distributed RAM (Kbits)	520	780	1,520	4,200	380	820	1,240	1,580	2,280	1,500	2,400
	Block RAM/FIFO w/ECC (36Kbits each)	84	132	244	516	68	148	228	298	456	228	324
	Total Block RAM (Kbits)	3,024	4,752	8,784	18,576	2,448	5,328	8,208	10,728	16,416	8,208	11,664
Clock Resources	Digital Clock Managers (DCM)	4	12	12	12	4	12	12	12	12	12	12
	Phase Locked Loop (PLL)/PMOD	2	6	6	6	2	6	6	6	6	6	6
I/O Resources (4, 5)	Maximum Single-Ended Pins	360	480	640	960	360	640	680	840	960	680	680
	Maximum Differential I/O Pairs	180	240	320	480	180	320	340	420	480	340	340
	I/O Standards	HT, LVDS, LVDS6T, RSQS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II										
Embedded (6) Hard IP Resources	DSP48E Slices	192	288	640	1,056	64	128	256	320	384	80	96
	PowerPC® 440 Processor Blocks	—	—	—	—	1	1	2	2	2	—	—
	PCI Express® Endpoint Blocks	1	1	1	1	1	3	3	3	4	1	1
	10/100/1000 Ethernet MAC Blocks	4	4	4	4	4	4	4	6	8	4	4
	RocketIO™ GTP Low-Power Transceivers	8	12	16	24	—	—	—	—	—	—	—
	RocketIO™ GTX High-Speed Transceivers	—	—	—	—	8	16	16	20	24	40	48
Speed Grades	Commercial	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2
	Industrial	-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2
Configuration	Configuration Memory (Mbits)	13.4	20.0	35.8	79.7	13.6	27.1	39.4	49.3	70.9	43.4	65.8
Package (7)		Area		Available User I/O: SelectIO Interface Pins (GTP/GTX Serial Transceivers)								
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)												
	FF324	19 x 19 mm										
	FF676	27 x 27 mm										
	FF1153	35 x 35 mm										
	FF1760	42.5 x 42.5 mm										
	FF323	19 x 19 mm										
	FF665	27 x 27 mm	360 (8)	360 (8)		360 (8)	360 (8)					
	FF1136	35 x 35 mm		480 (12)	640 (16)		640 (16)					
	FF1738	42.5 x 42.5 mm				960 (24)		680 (16)	840 (20)	960 (24)		
	FF1156	35 x 35 mm									360 (40)	
	FF1759	42.5 x 42.5 mm									680 (40)	680 (48)

- Notes:
1. EasyPath™ solutions provide a conversion-free and low risk path for volume production.
 2. A single Virtex-5 FPGA comprises two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
 3. Virtex-5 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
 4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
 5. I/O standards supported HT, LVDS, LVDS6T, RSQS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II
 6. One system monitor block included in all devices.
 7. All products available Pb-free and RoHS-Compliant.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com/virtex5

Virtex-4 Family FPGAs



		Virtex-4 LX FPGAs Optimized for High-performance Logic (1.2 Volt)							Virtex-4 SX FPGAs Optimized for DSP (1.2 Volt)			Virtex-4 FX FPGAs Optimized for Embedded Processing & Serial Connectivity (1.2 Volt)						
Part Number		XC4VLX15	XC4VLX25	XC4VLX40	XC4VLX60	XC4VLX80	XC4VLX100	XC4VLX160	XC4VLX200	XC4VSX25	XC4VSX35	XC4VSX55	XC4VFX12	XC4VFX20	XC4VFX40	XC4VFX60	XC4VFX100	XC4VFX140
EasyPath™ Cost Reduction Solutions ⁽¹⁾		—	—	XCE4VLX40	XCE4VLX60	XCE4VLX80	XCE4VLX100	XCE4VLX160	XCE4VLX200	—	XCE4VSX35	XCE4VSX55	—	—	XCE4VFX40	XCE4VFX60	XCE4VFX100	XCE4VFX140
Logic Resources	Slices ⁽²⁾	6,144	10,752	18,432	26,624	35,840	49,152	67,584	89,088	10,240	15,360	24,576	5,472	8,544	18,624	25,280	42,176	63,168
	Logic Cells	13,824	24,192	41,472	59,904	80,640	110,592	152,064	200,448	23,040	34,560	55,296	12,312	19,224	41,904	56,880	94,896	142,128
	CLB Flip-Flops	12,288	21,504	36,864	53,248	71,680	98,304	135,168	178,176	20,480	30,720	49,152	10,944	17,088	37,248	50,560	84,352	126,336
Memory Resources	Maximum Distributed RAM (Kbits)	96	168	288	416	560	768	1,056	1,392	160	240	384	86	134	291	395	659	987
	Block RAM/FIFO w/ECC (18 Kbits each)	48	72	96	160	200	240	288	336	128	192	320	36	68	144	232	376	552
	Total Block RAM (Kbits)	864	1,296	1,728	2,880	3,600	4,320	5,184	6,048	2,304	3,456	5,760	648	1,224	2,592	4,176	6,768	9,936
Clock Resources	Digital Clock Managers (DCM)	4	8	8	8	12	12	12	12	4	8	8	4	4	8	12	12	20
	Phase-matched Clock Dividers (PMCD)	0	4	4	4	8	8	8	8	0	4	4	0	0	4	8	8	8
I/O Resources ^(3,4)	Maximum Single-Ended I/Os	320	448	640	640	768	960	960	960	320	448	640	320	320	448	576	768	896
	Maximum Differential I/O Pairs	160	224	320	320	384	480	480	480	160	224	320	160	160	224	228	384	448
	I/O Standards	LDT-25, LVDS-25, LVDSEXT-25, BLVDS-25, ULVDS-25, LVPECL-25, LVCMOS25, LVCMOS18, LVCMOS15, PCI33, LVTTL, LVCMOS33, PCI-X, PCI66, GTL, GTL+, HSTL I (1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2I, SSTL2II, SSTL18 I, SSTL18 II																
Embedded Hard IP Resources	DSP48 Slices	32	48	64	64	80	96	96	96	128	192	512	32	32	48	128	160	192
	PowerPC® Processor Blocks	—	—	—	—	—	—	—	—	—	—	—	1	1	2	2	2	2
	10/100/1000 Ethernet MAC Blocks	—	—	—	—	—	—	—	—	—	—	—	2	2	4	4	4	4
	RocketIO™ Serial Transceivers	—	—	—	—	—	—	—	—	—	—	—	0	8	12	16	20	24
Speed Grades	Commercial	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12
	Industrial	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11
Configuration	Configuration Memory (Mbits)	4.8	7.8	12.3	17.7	23.3	30.7	40.3	51.4	9.1	13.7	22.7	4.8	7.2	14.9	21.0	33.0	47.9
Package ⁽⁷⁾		Area																
		Available User I/O: SelectIO Interfaces Pins (RocketIO Transceivers)																
		SFA Packages (SF): flip-chip fine-pitch BGA (0.8 mm ball spacing)																
SF363	17 x 17 mm	240	240										240					
		FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)																
FF668	27 x 27 mm	320	448	448	448					320	448		320					
FF1148	35 x 35 mm			640	640	768	768	768			640							
FF1513	40 x 40 mm						960	960	960									
FF672	27 x 27 mm												320 (8)	352 (12)	352 (12)			
FF1152	35 x 35 mm													448 (12)	576 (16)	576 (20)		
FF1517	40 x 40 mm															768 (20)	768 (24)	

- Notes: 1. EasyPath™ solutions provide a conversion-free and low-risk path for volume production.
 2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
 3. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
 4. I/O standards supported HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II
 5. All Virtex-4 LX and Virtex-4 SX devices available in the same package are footprint-compatible.
 6. All products available Pb-free and RoHS-Compliant.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com/virtex4