Smart NIC Cloud Acceleration

Providing Service-Driven Data Center Networking

RAYMAX 锐文科技 XILINX

XILINX ALVEO™

- 100GE
- P4-enabled, with P4 compiler
- Virtual Switch Data plane Offload
- Network Accelerator

INTRODUCTION

With the ever-increasing growth of cloud services, thanks to the emerging 5G technologies, crypto, scalable micro-service architecture, machine learning analytics and so on, high performance network and computational infrastructure is of a necessity. The most challenging matter for today Data Centers, apart from hosting diverse range of applications, is to quickly serve big volumes of the requests in scale of millions. The performance of these applications perceived by end users is being dominated by server latency and bandwidth. Server end network processing in low to medium speeds (<10G) is still well possible exploiting native OS drivers and powerful multicore processors available in the market. However, to achieve high bit rate (>25G), servers need to use technologies such as kernel bypass and offloading to be able to reach the high throughputs without using the CPU cycles out of proportion.
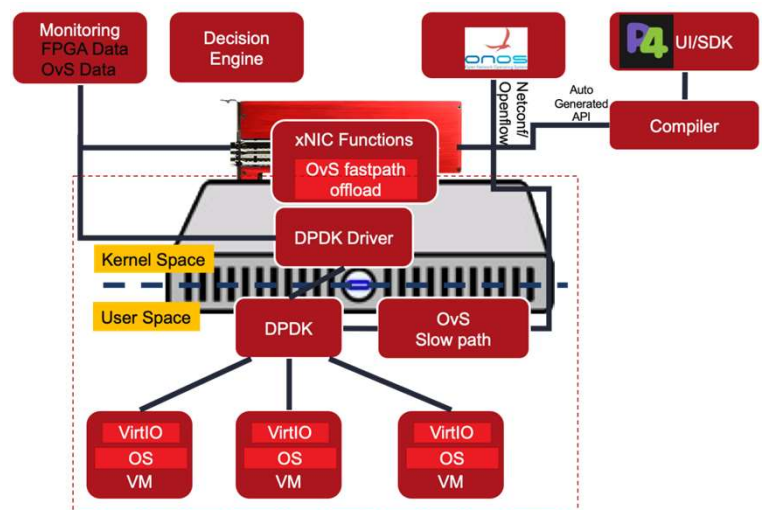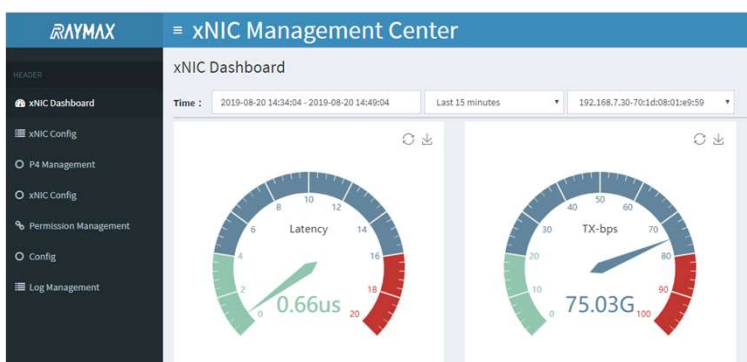
KEY BENEFITS

- Accelerate the server end networking
- Offloading CPU
- Service driven data plane programmability
- Reduce CAPEX and OPEX

SOLUTION OVERVIEW

XILINX

Adaptable. Intelligent.

SOLUTION DETAILS

Raymax Smart NIC solution is designed for web-scale cloud and networking requirements. By leveraging the open standards, platforms and software-defined approaches, we supply a white box Smart NIC solution from software to hardware to offload the CPU and respond to the real time data center networking service request.
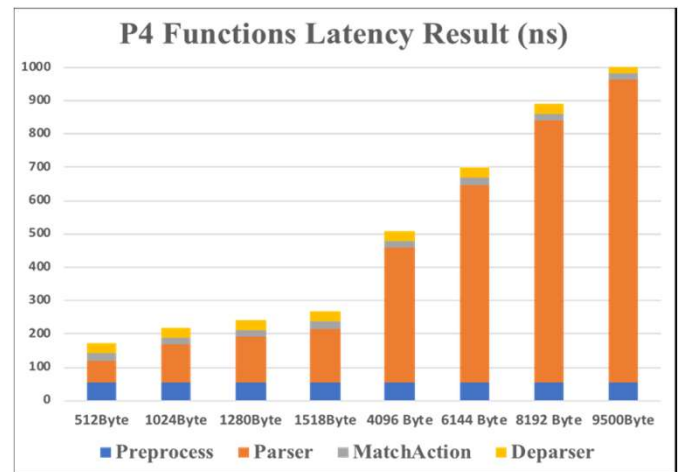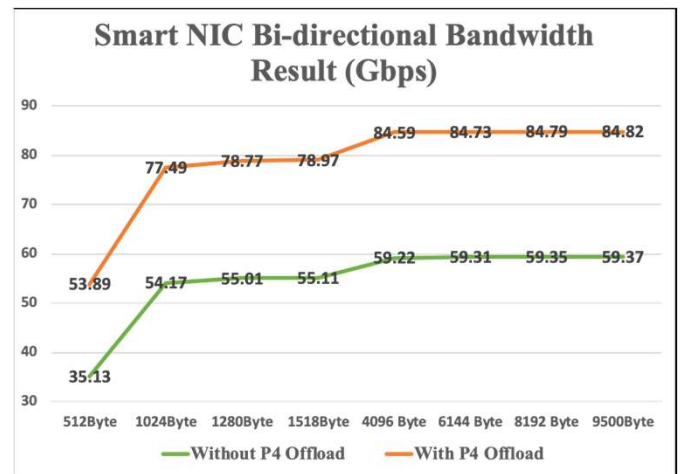
The solution includes software part and FPGA-based data plane part. On the software side (a), we supplied the Linux kernel driver and DPDK driver to accommodate our FPGA-based Smart NIC. For data modelling and registry of hardware and software resources/services, it is SDN ready (OpenFlow, P4Runtime) as well as supporting legacy network management systems (NETCONF, SNMP). In addition, we supplied the GUI-based P4 compiler which is compatible to our back end devices. On the hardware side (b), the FPGA-based programmable data plane is designed as service-driven path supporting P4 and virtual Switch fast data path for CPU offload and multiple-VM applications.

RESULTS

The bandwidth result was measured with 1 CPU core in the PC of Intel Core i7-7700K CPU @ 4.20GHz x8, 62.8GiB Memory hardware setup. We inserted one SR-MPLS header to the packet and measured the maximum bandwidth of inserting by software (Without P4 SR-MPLS Offload) and inserting by FPGA (With P4 SR-MPLS Offload). The result demonstrated, with offload, the Smart NIC was able to achieve maximum 78.97Gbps throughput with 1518 Ethernet frame size and could go up to 84.82Gbps with jumbo frame size. Without offload, the bandwidth went down maximum 30%.

The latency result revealed the detail nanosecond latency of each functional block in the FPGA.

TAKE THE NEXT STEP

Learn more about Xilinx Alveo accelerator cards
Learn more about Partner Raymax Technology
Reach out to Raymax sales – sales@raymax.net

a

b

Smart NIC Bi-directional Bandwidth Result (Gbps)

P4 Functions Latency Result (ns)

Adaptable. Intelligent.