CoolRunner-II CPLD

Increased System Performance

- Delivers high performance with low power
- DualEDGE flip-flop capability
- Guaranteed I/O-to-I/O timing

Total Power Reduction

- 1.8V all-digital core with Fast Zero Power technology
- DataGATE signal blocking and CoolCLOCK technology reduces dynamic power
- Ultra-low power (28.8µW)
- Industry's lowest standby current (16µA typical) without power-down modes

BOM Cost Reduction

- 2 to 4 I/O banks for voltage integration
- Input hysteresis and programmable grounds
- Multiple LVCMOS, HSTL, SSTL I/O
- On-the-fly reconfiguration
- Small, low-cost QF32 and QF48 packages
- Four-level design security averts pattern theft

Total Power Reduction

- Up to 50% lower power vs. 7 series FPGAs
- Voltage scaling options for performance and power
- Tighter logic cell packing reduces dynamic power

Small Form Factor Packaging for I/O Connectivity

- 32-macrocell device in 5x5mm packaging
- Suitable for handheld and other space constrained applications
- Can be used as glue logic across multiple industries

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CoolRunner™-II

Industry's Best Single-Chip, Instant-On CPLDs

The CoolRunner™-II 1.8V family provides the industry's highest performance low-power CPLD in a nonvolatile technology. Enhanced with revolutionary features such as DataGATE, advanced I/Os and the industry's smallest form factor packaging, CoolRunner-II CPLDs deliver the ultimate system solution for today's design challenges.

Enabled by Second-Generation Fast Zero Power (FZP) Technology

Fast Zero Power (FZP) is the patented design technology used in CoolRunner-II devices for high-speed, low power programmable logic. Unlike sense amplifiers found in other CPLDs, Fast Zero Power represents a programmable logic breakthrough that minimizes system current demand and allows small chip-scale package options. Fast Zero Power uses minimal standby current, without restricting power limits on device size, while providing both high performance and low power. Low power designs are enabled through FZP by using true CMOS both in process technology and design technique.

Features	
Fast Zero Power Technology	• High performance and low power • Lowest standby current available in a CPLD (as low as 12µA)
Lower CPLD Operating & System Power	• Patented DataGATE feature stops unwanted input switching from continuously draining power • CoolCLOCK is a combination of the clock divider and doubler
Advanced I/O Support with Guaranteed I/O-to-I/O Timing	• Includes SSTL and HSTL • Flexible output banking
Small Form Factor, Lowest-Cost Packaging	• Industry's smallest form factor 5x5mm QF CPLD package, for 32-macrocell device • Other 6x6mm, 7x7mm, and 8x8mm options available • Ideal for handheld & other constrained applications

CoolRunner™-II CPLDs

High performance and ultra-low power consumption in a single-chip, instant-on programmable device (1.8V)

	Part Number	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
Logic Resources	System Gates	750	1,500	3,000	6,000	9,000	12,000
	Macrocells	32	64	128	256	384	512
	Product Terms Per Macrocell	56	56	56	56	56	56
Clock	Global Clocks	3	3	3	3	3	3
	Product Term Clocks Per Function Block	16	16	16	16	16	16
I/O Resources	Maximum I/O	33	64	100	184	240	270
	Input Voltage Compatible	1.5 / 1.8 / 2.5 / 3.3					
	Output Voltage Compatible	1.5 / 1.8 / 2.5 / 3.3					
	Min. Pin-to-Pin Logic Delay (ns)	3.8	4.6	5.7	5.7	7.1	7.1
Speed Grades	Commercial Speed Grades (Fastest to Slowest)	-4, -6	-5, -7	-6, -7	-6, -7	-7, -10	-7, -10
	Industrial Speed Grades (Fastest to Slowest)	-6	-7	-7	-7	-10	-7[1], -10

Package[3], [4]	Area (mm)			Maximum User I/Os			
QFN Packages (QF): Quad, flat, no-lead (0.5mm lead spacing)							
QFG32[4]	5 x 5	21					
QFG48[4]	7 x 7		37				
VQFP Packages (VQ): Very thin QFP (VQ44: 0.8mm lead spacing, VQ100: 0.5mm lead spacing)							
VQG44	12 x 12	33	33				
VQG100	16 x 16		64	80	80		
Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5mm ball spacing)							
CPG56	6 x 6	33	45				
CPG132	8 x 8			100	106		
TQFP Packages (TQ): Thin QFP (0.5mm lead spacing)							
TQG100	16 x 16						
TQG144	22 x 22			100	118	118	
PQFP Packages (PQ): Wire-bond, plastic, QFP (0.5 mm lead spacing)							
PQG208	30.6 x 30.6 mm				173	173	173
FBGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)							
FTG256	17 x 17 mm				184	212	212
FBGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)							
FGG324	23 x 23 mm					240	270

Notes:

1. -7 speed grade is only available in FT(G)256 package.
2. All packages are available in Pb-Free and RoHS6 compliant versions.
3. Area dimensions for lead-frame product are inclusive of the leads.
4. Only available in RoHS6 compliant and Halogen-free packages.

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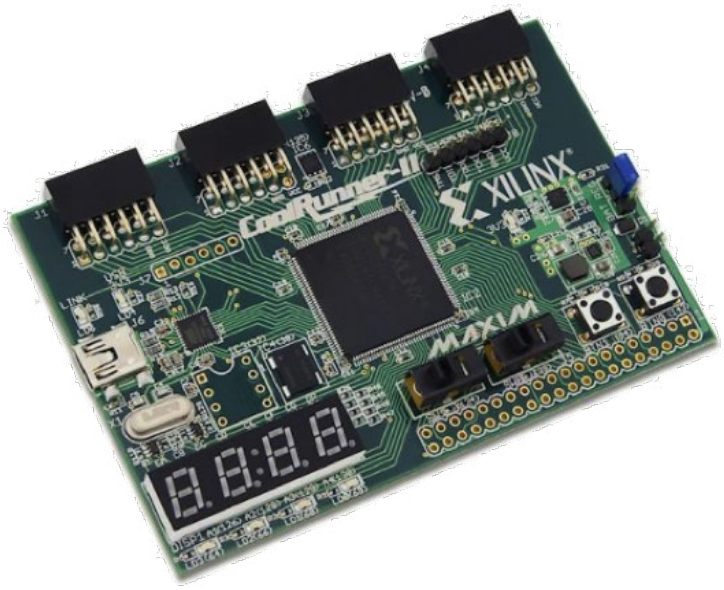

Digilent CoolRunner-II Evaluation Kit

A complete toolbox to help designers develop the latest CPLD designs for under $40.

The Digilent CoolRunner-II CPLD starter board is the ideal platform for the evaluation and implementation of designs using a high-performance, low-power CPLD. Targeted applications include intelligent handheld devices, remote monitoring, wireless interfacing, and glue logic across any number of industries.

The DataGATE switch allows designers to easily evaluate a unique power option that permits input signal blocking, stops input switching, and significantly reduces power consumption, thereby extending battery life. With four 12-pin Pmod ports, you can easily add functions such as analog-to-digital conversion, servo motor interface, serial flash, RS-232 serial channel, accelerometers, temperature sensors, and more.

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