XILINX SPARTAN®-3, 3E FPGAS

			Spartan-3 FPGAs Optimized for High-Density and High I/O Designs								Spartan-3E FPGAs Logic Optimized				
	Part Number		XC3S50	XC3S200	XC3S400	XC3S1000	XC3S1500	XC3S2000	XC3S4000	XC3S5000	XC3S100E	XC3S250E	XC3S500E	XC3S1200E	XC3S1600E
Logic Resources	System Gates[1]		50K	200K	400K	1,000K	1,500K	2,000K	4,000K	5,000K	100K	250K	500K	1,200K	1,600K
	Slices[2]		768	1,920	3,584	7,680	13,312	20,480	27,648	33,280	960	2,448	4,656	8,672	14,752
	Logic Cells		1,728	4,320	8,064	17,280	29,952	46,080	62,208	74,880	2,160	5,508	10,476	19,512	33,192
	CLB Flip-Flops		1,536	3,840	7,168	15,360	26,624	40,960	55,296	66,560	1,920	4,896	9,312	17,344	29,504
Memory Resources	Maximum Distributed RAM (Kb)		12	30	56	120	208	320	432	520	15	38	73	136	231
	Block RAM (18 Kb each)		4	12	16	24	32	40	96	104	4	12	20	28	36
	Total Block RAM (Kb)		72	216	288	432	576	720	1,728	1,872	72	216	360	504	648
Clock Resources	Digital Clock Managers (DCMs)		2	4	4	4	4	4	4	4	2	4	4	8	8
I/O Resources	Maximum Single-Ended I/Os		124	173	264	391	487	565	633	633	108	172	232	304	376
	Maximum Differential I/O Pairs		56	76	116	175	221	270	300	300	40	68	92	124	156
	I/O Standards Supported		LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, GTL, GTL+, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, Bus LVDS, LDT (ULVDS), LVDS_ext, LVDS25 & 33, LVPECL25, and RSDS25								LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL18 Class I, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, PCI 3.3V 64bit/66MHz, SSTL2 Class I, SSTL18 Class I, Bus LVDS, LVDS25, LVPECL25, Mini-LVDS25, RSDS25				
Embedded Hard IP Resources	Dedicated Multipliers		4	12	16	24	32	40	96	104	4	12	20	28	36
Speed Grades	Commercial		-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5
	Industrial		-4	-4	-4	-4	-4	-4	-4	-4	-4	-4	-4	-4	-4
Configuration	Configuration Memory (Mb)		0.4	1	1.7	3.2	5.2	7.7	11.3	13.3	0.6	1.4	2.3	3.8	6
	Package	Footprint Size	Maximum User I/Os												
	VQFP Packages (VQ): Very thin QFP (0.5 mm lead spacing)														
	VQ100	16 x 16 mm	63	63							66	66	66		
	Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5 mm ball spacing)														
	CP132	8 x 8 mm	89								83	92	92		
	TQFP Packages (TQ): Thin QFP (0.5 mm lead spacing)														
	TQ144	22 x 22 mm	97	97	97						108	108			
	PQFP Packages (PQ): Wire-bond, plastic, QFP (0.5 mm lead spacing)														
	PQ208	30.6 x 30.6 mm	124	141	141							158	158		
	FGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)														
	FT256	17 x 17 mm		173	173	173						172	190	190	
	FGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)														
	FG320	19 x 19 mm			221	221	221						232	250	250
	FG400	21 x 21 mm												304	304
	FG456	23 x 23 mm			264	333	333	333							
	FG484	23 x 23 mm													376
	FG676	27 x 27 mm				391	487	489	489	489					
	FG900	31 x 31 mm						565	633	633					

XMP072 (v1.1)

Notes: 1. System gates include 20%–30% of CLBs used as RAMs.

2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.

3. All products are available Pb-free and RoHS-Compliant.

4. Available only in VQG100 package. VQG100 and VQ100 have identical pinouts.

XILINX EXTENDED SPARTAN®-3A FPGAS

Extended Spartan-3A Family
Optimized for Lowest Total Cost

	Part Number		XC3S50A/AN	XC3S200A/AN	XC3S400A/AN	XC3S700A/AN	XC3S1400A/AN	XC3SD1800A	XC3SD3400A
Logic Resources	System Gates[1]		50K	200K	400K	700K	1400K	1800K	3400K
	Slices[2]		704	1,792	3,584	5,888	11,264	16,640	23,872
	Logic Cells		1,584	4,032	8,064	13,248	25,344	37,440	53,712
	CLB Flip-Flops		1,408	3,584	7,168	11,776	22,528	33,280	47,744
Memory Resources	Maximum Distributed RAM (Kb)		11	28	56	92	176	260	373
	Block RAM (18 Kb each)		3	16	20	20	32	84	126
	Total Block RAM (Kb)		54	288	360	360	576	1,512	2,268
Non-Volatile Capability	Single Chip Option		Yes	Yes	Yes	Yes	Yes	No	No
	User Flash (Kb)[3]		- / 627	- / 3,054	- / 2,380	- / 5,779	- / 12,251	—	—
Clock Resources	Digital Clock Managers (DCMs)		2	4	4	8	8	8	8
I/O Resources	Maximum Single-Ended I/Os		144 / 144	248 / 195	311	372	502	519	469
	Maximum Differential I/O Pairs		64 / 64	112 / 90	142	165	227	227	213
	I/O Standards Supported		LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, PCI 3.3V 64bit/66MHz, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25 & 33, LVPECL25 & 33, Mini-LVDS25 & 33, RSDS25 & 33, TMDS33, and PPDS25 & 33						
Embedded Hard IP Resources	Multipliers/DSP48A Blocks		3	16	20	20	32	84[4]	126[4]
	Device DNA Security		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Speed Grades	Commercial		-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5
	Industrial		-4	-4	-4	-4	-4	-4	-4
Configuration	Configuration Memory (Mb)		0.4	1.2	1.9	2.7	4.8	8.2	11.7
	Package[6]	Footprint Size	Maximum User I/Os						
	VQFP Packages (VQ): Very thin QFP (0.5 mm lead spacing)								
	VQ100	16 x 16 mm	68 / - [7]	68 / - [7]					
	TQFP Packages (TQ): Thin QFP (0.5 mm lead spacing)								
	TQ144	22 x 22 mm	108 / 108						
	BGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)								
	FT256	17 x 17 mm	144 / 144	195 / 195	195 / 195	161 / - [7]	161 / - [7]		
	Chip Scale Packages (CS): Wire-bond, chip-scale, BGA (0.8 mm ball spacing)								
	CS484	19 x 19 mm						309 [5]	309 [5]
	BGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)								
	FG320	19 x 19 mm		248 / - [7]	251 / - [7]				
	FG400	21 x 21 mm			311 / 311	311 / - [7]			
	FG484	23 x 23 mm				372 / 372	375 / 375		
	FG676	27 x 27 mm					502 / 502	519	469

XMP072 (v1.1)

Notes:
1. System gates include 20%–30% of CLBs used as RAMs.
2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
3. Spartan-3AN User Flash is the remaining storage capacity in the on-chip flash after storing the configuration bitstream.
4. Integrated in the DSP48A slices (Advanced Multiply Accumulate element).
5. The low-power option is exclusively available in CS(G)484 package and Industrial temperature range.
6. All products are Pb-free and RoHS-Compliant; check data sheet for Pb package availability.
7. Package is not available in nonvolatile Spartan-3AN family.