



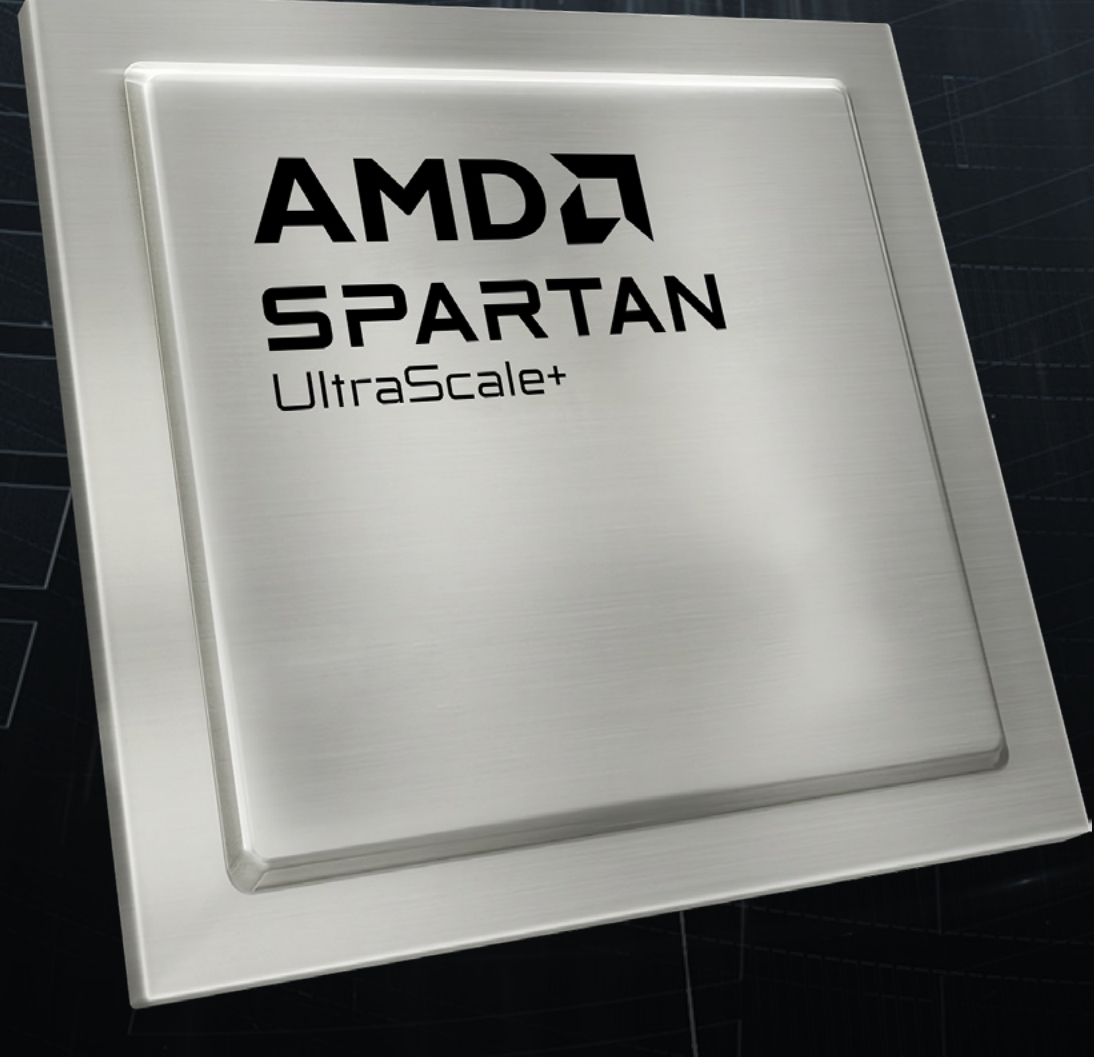
ACCELERATE TIME-TO-MARKET FOR COST-SENSITIVE DESIGNS

Introducing the new AMD Spartan™ UltraScale+™ FPGA family.

High I/O. Low Power. Robust Security Features.

304 I/O

at 11K logic cells



Up to a **30%**

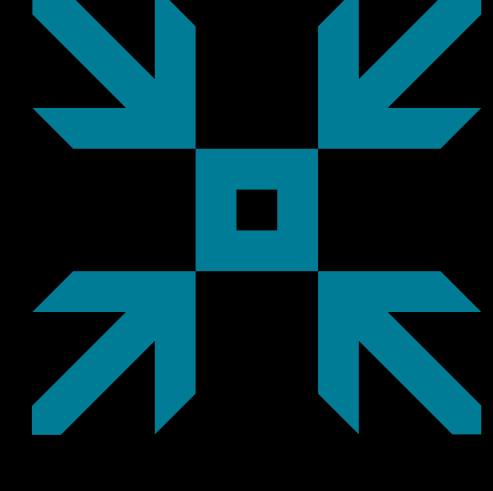
power reduction (projection)¹

572 I/O

at 218K logic cells

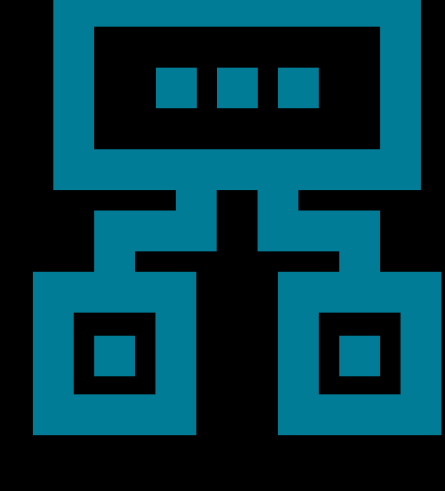
Security for a **post-quantum** age

More Features in a Smaller Package



SAVE SPACE AND REDUCE COMPLEXITY

- Industry's highest I/O-to-logic-cell ratio ≤ 28 nm process²
- 9 devices, 16 nm architecture
- Packaging options as small as 10x10 mm



TAP INTO ADVANCED CONNECTIVITY OPTIONS

- Hardened PCIe® Gen4, DDR memory controller
- 16.3 Gb/s GTH transceivers
- MIPI D-PHY up to 3.2 Gb/s

Ideal for Power-Constrained Environments

I/O EXPANSION

BOARD MANAGEMENT AND CONTROL

SENSING AND CONTROL

INDUSTRIAL EDGE

Easy-to-Use Design Software



Create, integrate, and implement designs with an intuitive, **all-in-one tool**.

40 Years of Innovation

EXPLORE A PORTFOLIO FROM THE INDUSTRY'S PROVEN PARTNER

COST-OPTIMIZED

Providing features and affordability

POWER-EFFICIENT

Delivering performance with low power

SMALL FORM FACTOR

Balancing physical size and logic requirements



AMD Spartan UltraScale+ Device Family

Achieve rapid time-to-market for cost-sensitive, I/O-intensive applications.

Meet the Family

¹ Projection is based on AMD labs internal analysis in January 2024, using Total Power calculation (Static plus Dynamic power) based on the difference in logic cell count of an AMD Artix™ UltraScale+ AL7P FPGA, to estimate the power of a 16 nm AMD Spartan™ UltraScale+ S15SP FPGA versus a 28 nm AMD Artix 7 7A33T FPGA, using Xilinx Power Estimator (XPE) tool version 2023.1.2. Actual Total Power will vary when final products are released in market, based on configuration, design, usage, and other factors. (SUS-03)

² Based on product data sheets for AMD Spartan™ UltraScale+™ FPGAs versus Efinix, Intel, Lattice, and Microchip, as of February 2024, comparing the total I/O-to-logic-cell ratios of comparable 28 nm and lower node size FPGAs. (SUS-10)

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