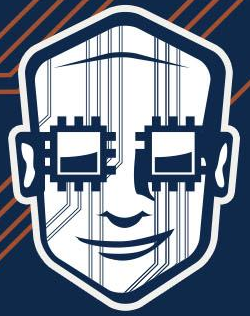
DesignCon® 2015



ULTRASCALE DDR4 DE-EMPHASIS AND CTLE FEATURE OPTIMIZATION WITH STATISTICAL ENGINE FOR BER SPECIFICATION

XILINX ALL PROGRAMMABLE.

KEYSIGHT TECHNOLOGIES

UBM Tech

Penglin Niu, penglin@xilinx.com

Fangyi Rao, fangyi_rao@keysight.com

Juan Wang, juanw@xilinx.com

Gary Otonari, gary_otonari@keysight.com

Nilesh Kamdar, nilesh_kamdar2@keysight.com

Yong Wang, yongw@xilinx.com

Outline

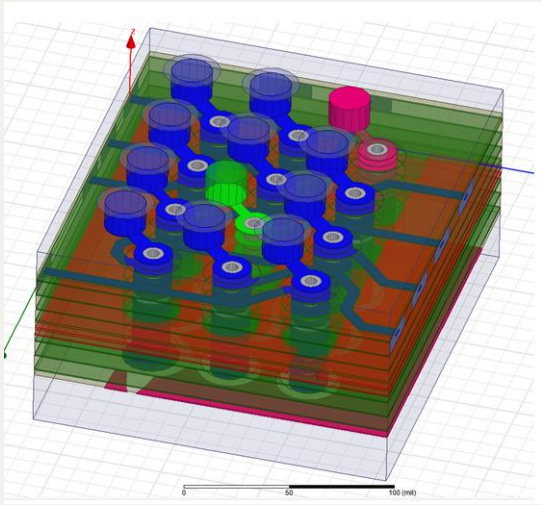
- DDR4 feature and design challenge
- FPGA DDR system design challenge
- DDR4 statistical simulation method
- DDR4 De-emphasis and CTLE optimization result discussion

DDR4 Features

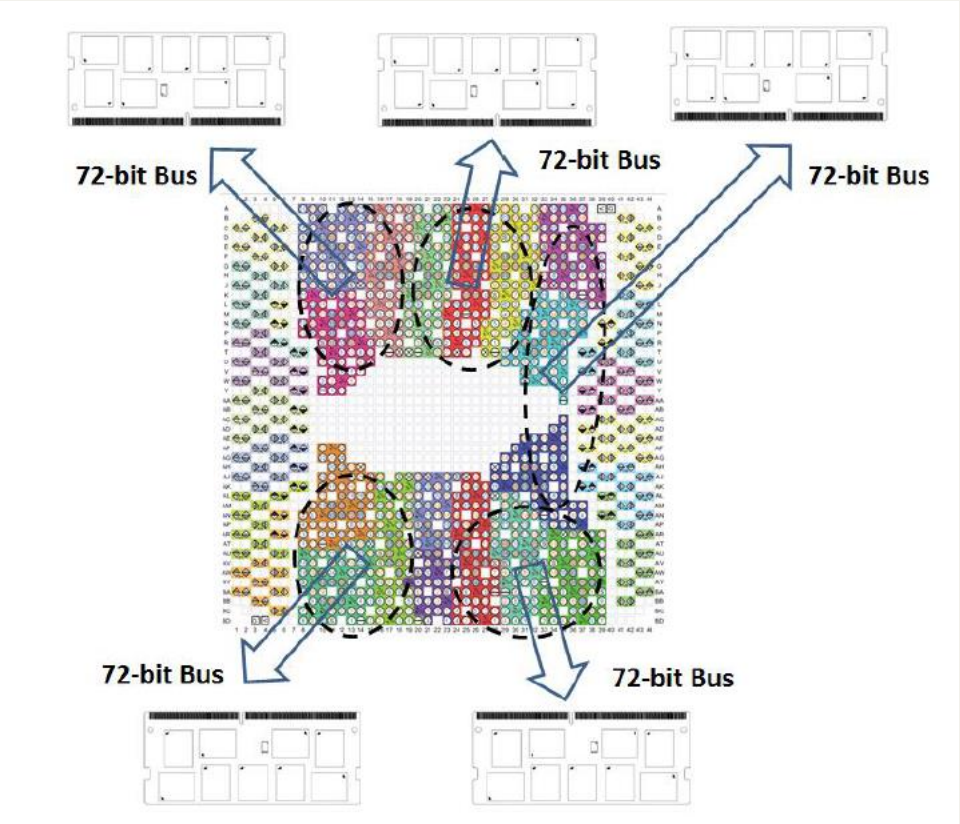
Feature	DDR3	DDR4
Voltage	1.5V	1.2V
Max Datarate (Mbps)	2133	3200
DQ Bus	SSTL15	POD12
DQ Vref	external	Internal
DQ Driver	40 (ohm)	48(ohm)

FPGA DDR4 Design Challenges

- **DDR4 Design Challenge**
  - Higher datarate, Higher loss, intensified ISI
- **FPGA Configurable I/O standards**
  - DDR3, DDR3L, DDR4, LPDDR2, LPDDR3, RLDRAM3, QDR2+, QDR4
  - High pad capacitance: FPGA ~3.5pF Vs. ~1.8pF ASIC
- **FPGA High I/O count**
  - Up to ~1400 IO counts in Ultrascale family
  - High density signal routing
  - High signal to ground ratio
- **Signal enhancement techniques to mitigate**
  - De-emphasis & CTLE

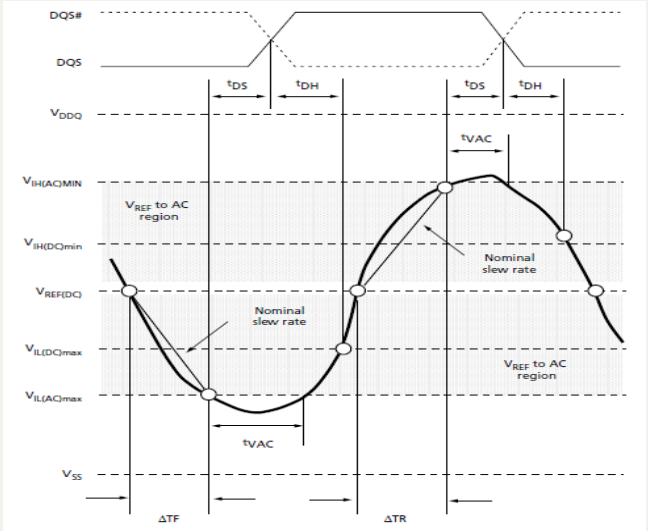


FPGA DDR4 Design Challenges



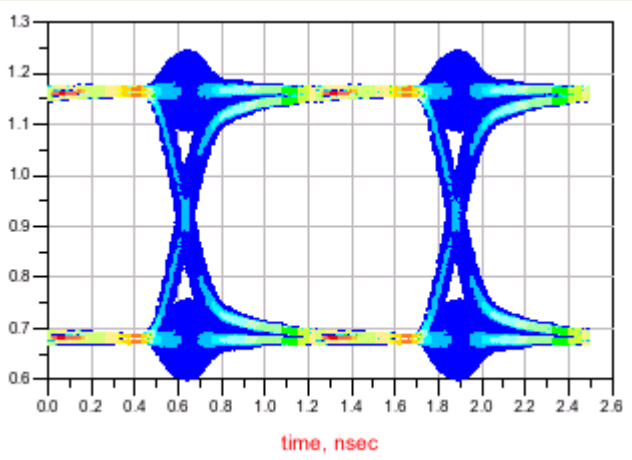
Traditional DDR Design Methodology

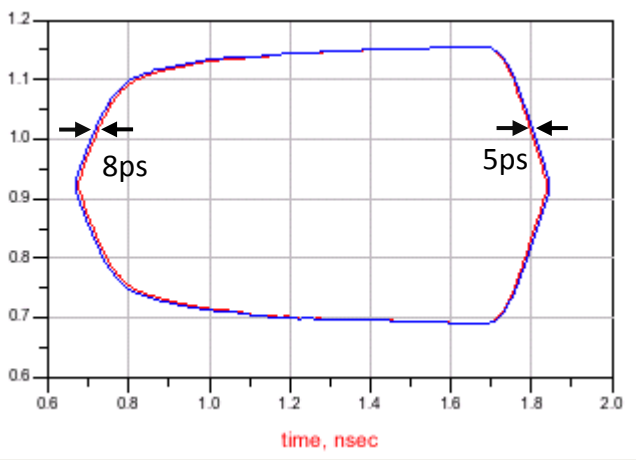
- Run transient simulation using IBIS or SPICE models of controller and memory
- Measure setup and hold times on waveforms



ISI at Low Speed

800 Mb/s





Border of traces of 10^3 bits

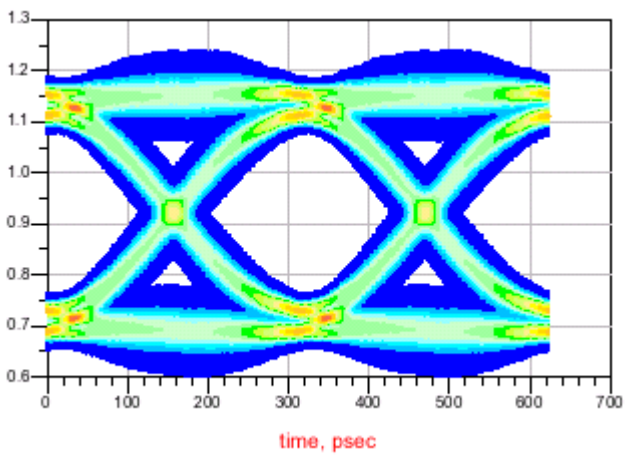
Border of traces of 10^{16} bits

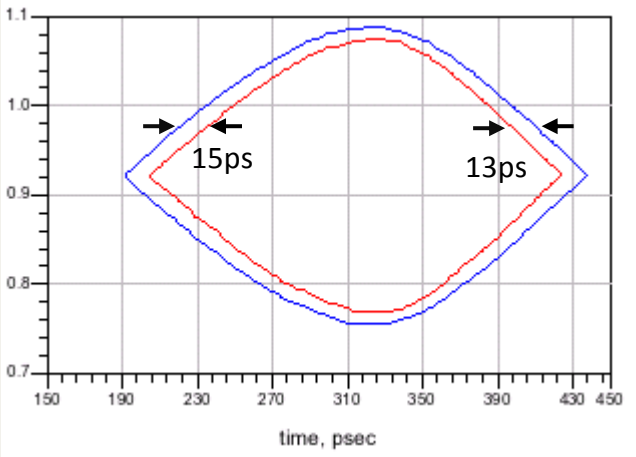
5” DQ line

- Timing margin deceases by 1% UI from 10^3 bits to 10^{16} bits
- At low speed, limited number of bits is adequate for system verification

ISI at High Speed

3200 Mb/s





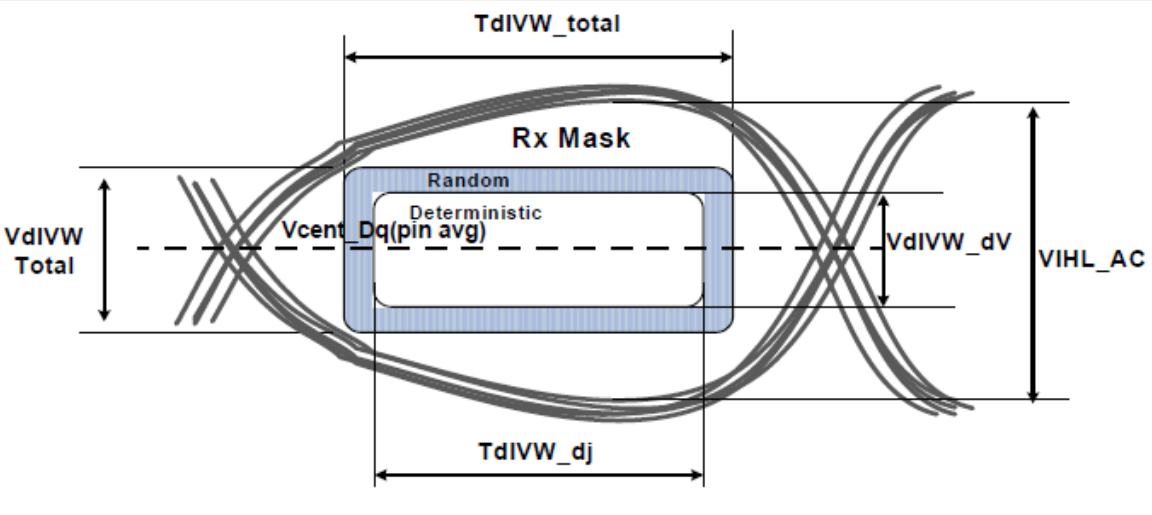
Border of traces of 10^3 bits

Border of traces of 10^{16} bits

5” DQ line

- Timing margin deceases by 9% UI from 10^3 bits to 10^{16} bits
- At high speed, design needs to be verified at target BER

DQ Rx Mask Spec in DDR4

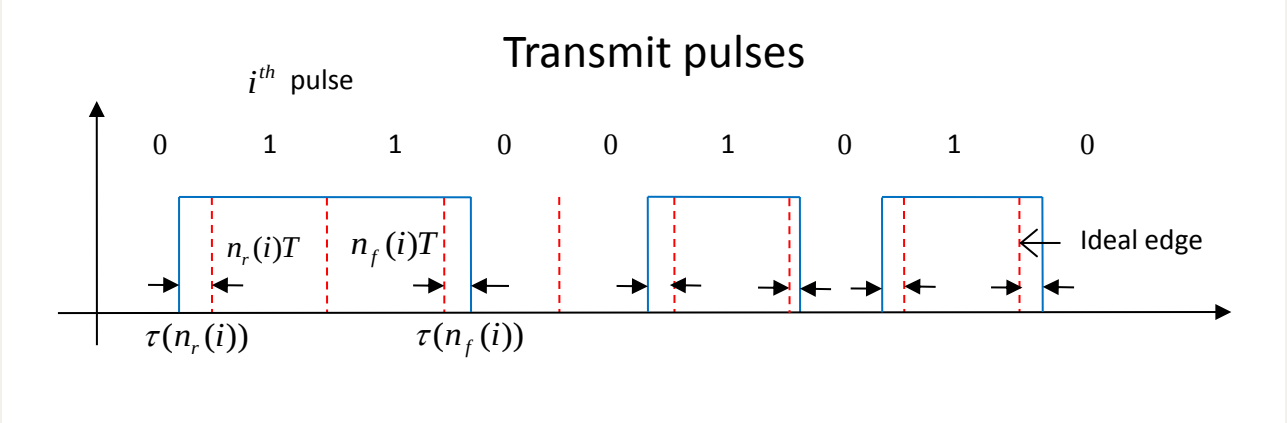


- Mask consists of deterministic and random portions
- BER inside the total mask must be below 10^{-16}

Statistical Simulation for BER

- It's impractical to simulate 10^{16} bits to estimate BER at 10^{-16}
- Statistical method can be employed to calculate eye probability distributions
- Equivalent to running infinite number of bits
- BER can be obtained rigorously at arbitrarily low level

Linear Superposition



$$v(t) = \sum_i \left\{ R[t - n_r(i) \cdot T - \tau(n_r(i))] - F[t - n_f(i) \cdot T - \tau(n_f(i))] \right\} + v_0$$

R(t): rise edge step response
F(t): fall edge step response
T: UI
τ : transmitter jitter

Transmitter Jitter

Jitter components include DCD, SJ and RJ

$$\tau(n_r) = -\frac{DCD_{pp}^{data}}{2} - (-1)^{n_r}\frac{DCD_{pp}^{clk}}{2} + Asin(2\pi f n_r T + \phi) + \rho(n_r)$$

$$\tau(n_f) = \frac{DCD_{pp}^{data}}{2} - (-1)^{n_f}\frac{DCD_{pp}^{clk}}{2} + Asin(2\pi f n_f T + \phi) + \rho(n_f)$$

DCD_{pp}^{data} : peak-to-peak data DCD

DCD_{pp}^{clk} : peak-to-peak clock DCD

A & f: SJ amplitude and frequency

ρ: RJ

Eye Probability Distribution

$$p(v,t) = \frac{1}{2\pi}\int_0^{2\pi} d\phi \frac{1}{2^M}\sum_{m=1}^{2^M}\int \delta[v - v^{(m)}(t)] \cdot \prod_i g[\rho(n_r^{(m)}(i))] \cdot g[\rho(n_f^{(m)}(i))] \cdot d\rho(n_r^{(m)}(i)) \cdot d\rho(n_f^{(m)}(i))$$

m: pattern index

M: step response settle time in bit

g: RJ PDF

- Tx jitter affects the output distribution through channel step responses
- Jitter effect is directly handled in PDF calculation instead of post-processing
- PDF is computed rigorously using efficient algorithms w/o approximation
- Accurate prediction of BER

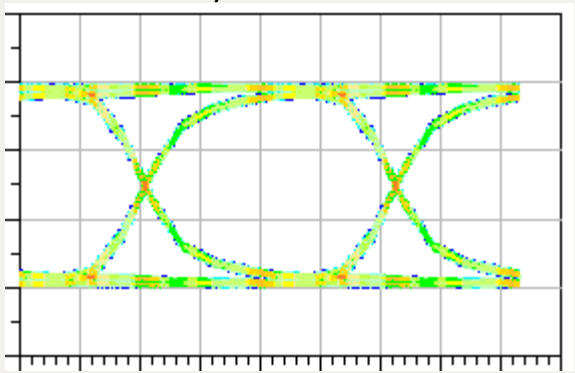
Crosstalk

Crosstalk is additive noise to victim signal

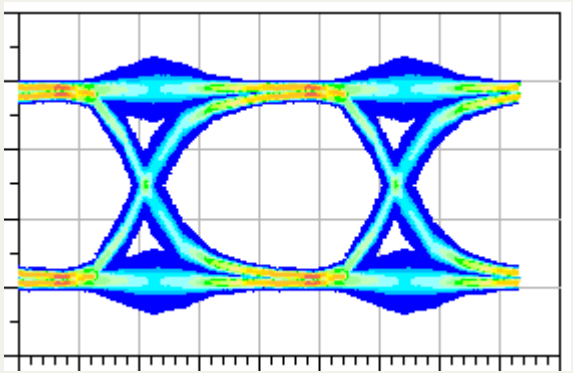
Included by convolution between victim PDF and crosstalk PDF

$$p(v,t) = \int p_{victim}(v - v_1 - v_2 \cdots - v_n, t)\, p_{xtlk}^{(1)}(v_1, t) p_{xtlk}^{(2)}(v_2, t) \cdots p_{xtlk}^{(n)}(v_n, t) dv_1 dv_2 \cdots dv_n$$

w/o crosstalk

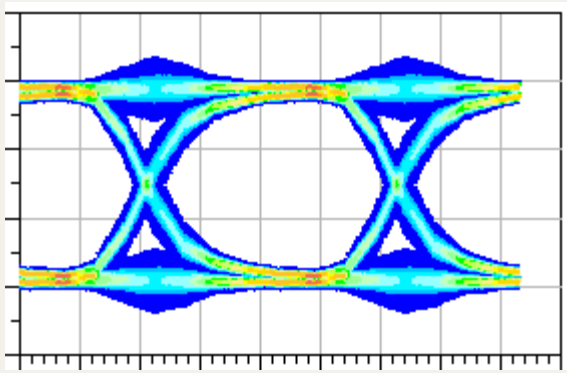


with crosstalk

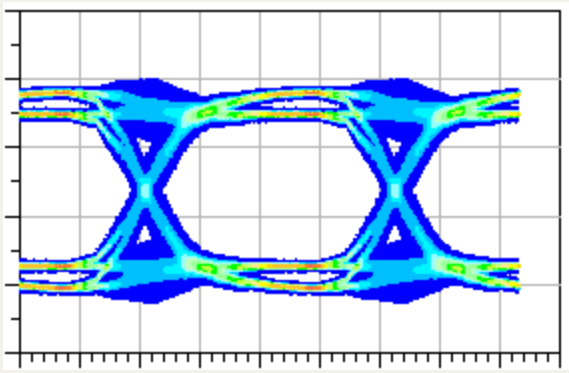


Driver De-emphasis

w/o de-emphasis

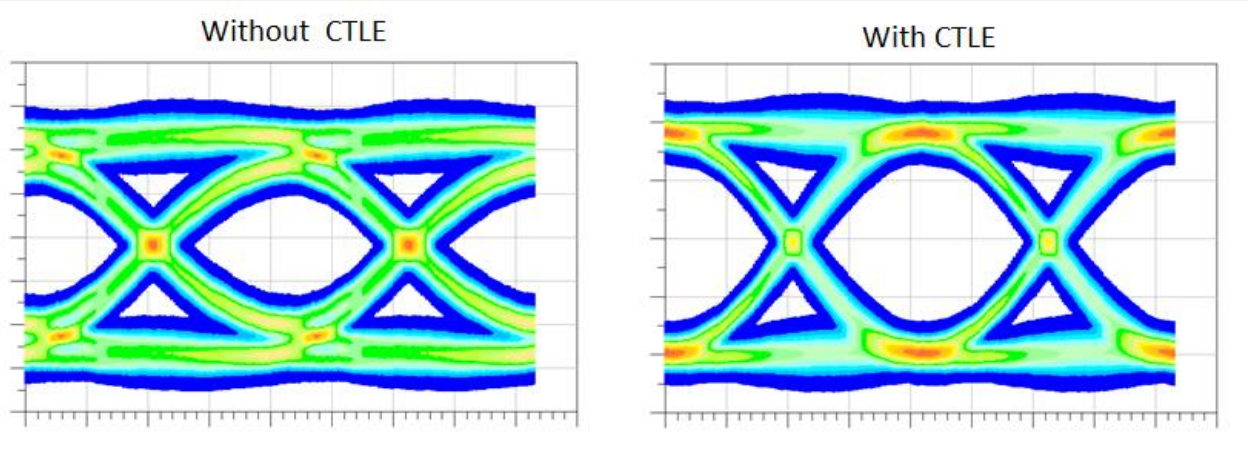


3dB de-emphasis



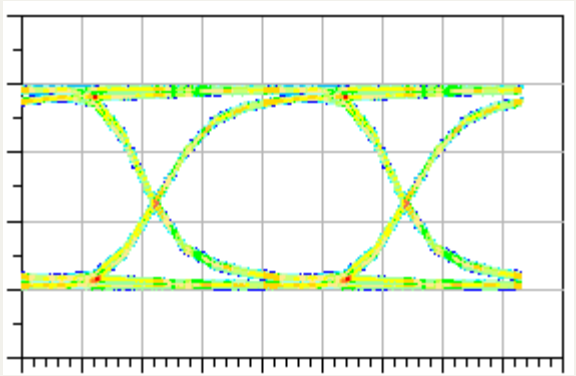
Rx CTLE

$$H(s) = A\frac{(s - z_1)\dots(s - z_n)}{(s - p_1)\dots(s - p_k)}$$

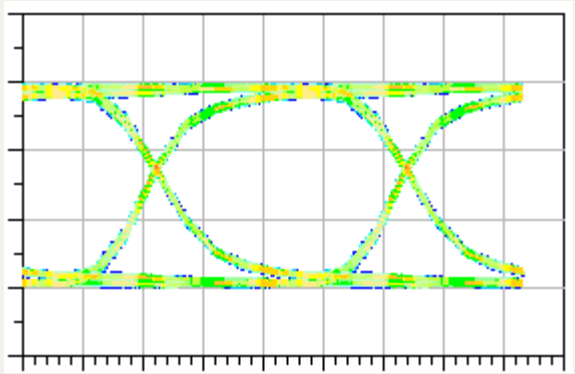


Asymmetric Rise and Fall Edges Capability

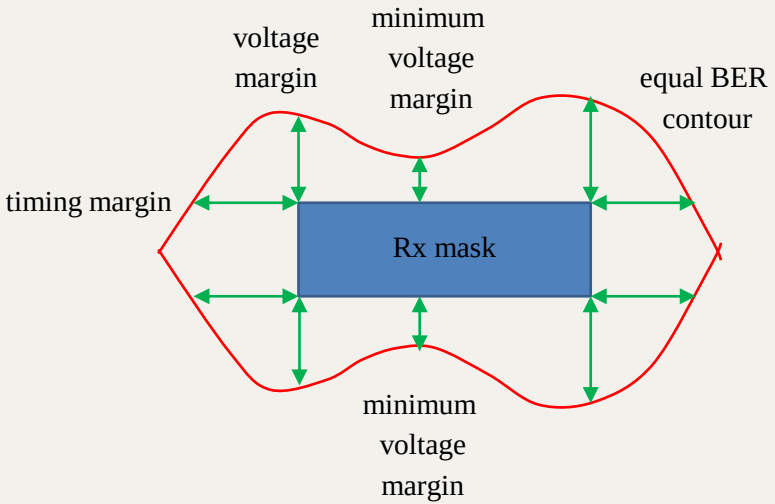
rise time > fall time



rise time < fall time

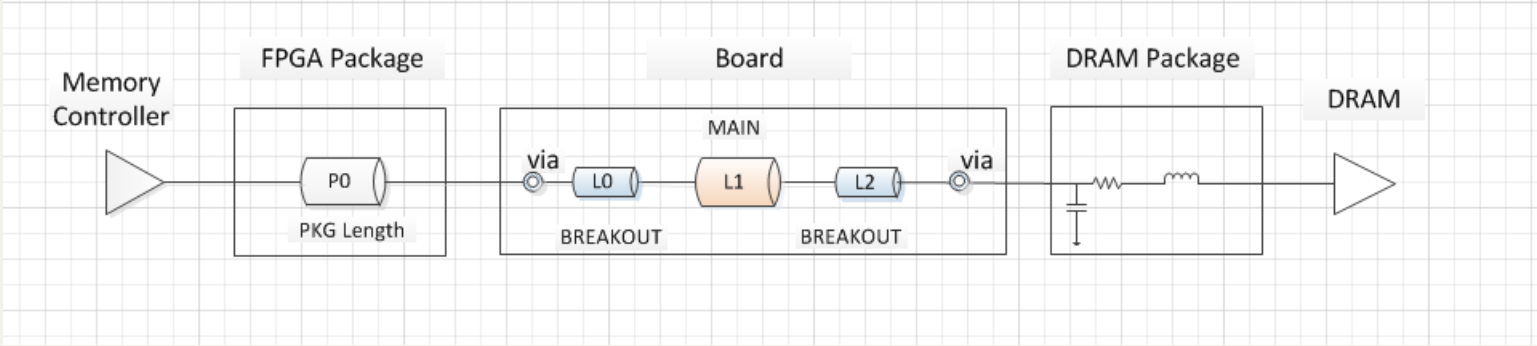


Timing and Voltage Margins



- Timing and Voltage margins are measured at each mask corner
- Ring-back is captured by minimum voltage margins

DDR4 Channel Topology



CTLE Optimization

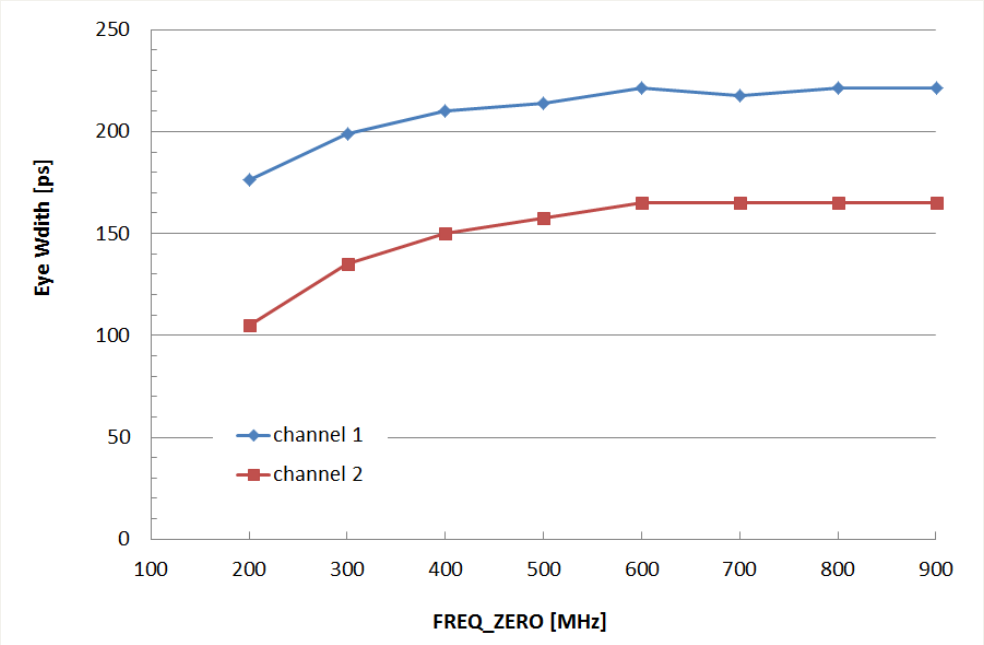
- CTLE design parameters
  - fz (zero), fp1 (first pole), fp2 (second pole), Gain_dc (dc gain)

$$H_{CTLE}(s) = c\frac{(s+w\_zero)}{(s+w\_pole1)(s+w\_pole2)}$$

$$c = Gain\_dc\frac{w\_pole1 * w\_pole2}{w\_zero}$$

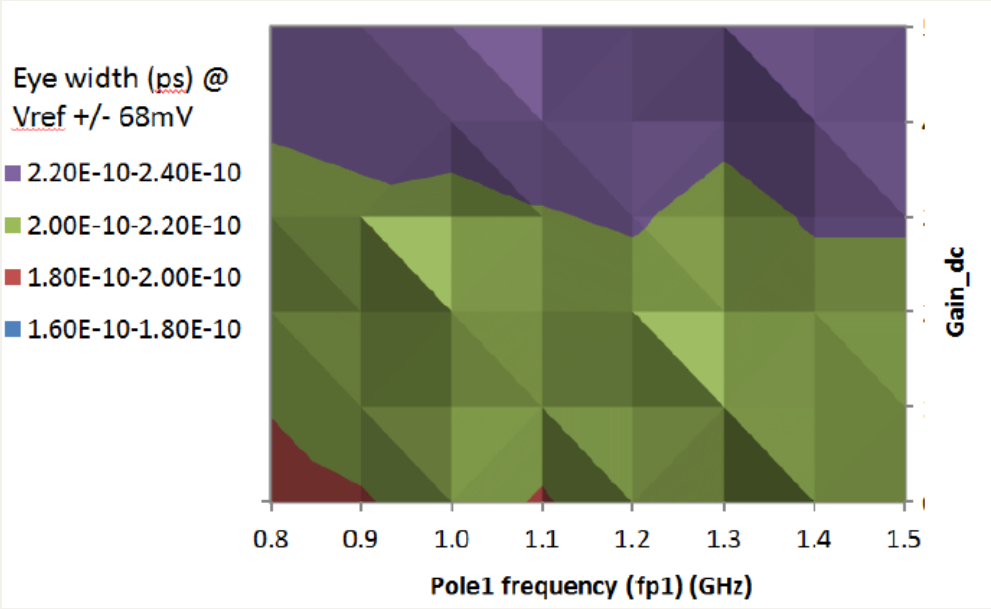
CTLE Optimization

- CTLE fz sensitivity sweep for two study channels
  - BER 10^{-16} eye width @ Vref +/-68mV saturated after 600Mhz fz



CTLE Optimization

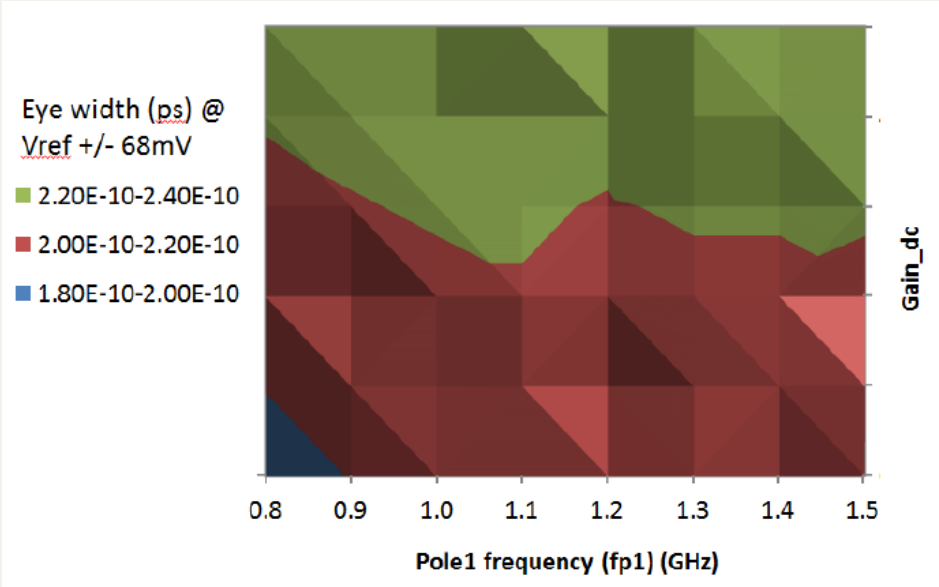
- CTLE fp1 Vs. Gain_dc sensitivity sweep at 4.5GHz bandwidth
  - BER 10^{-16} eye width not sensitive to fp1 around 1.2GHz
  - BER 10^{-16} eye width increase with higher Gain_dc



BER 10-16 eye width from fp1 and gain_dc at 4.5GHz bandwidth (fp2)

CTLE Optimization

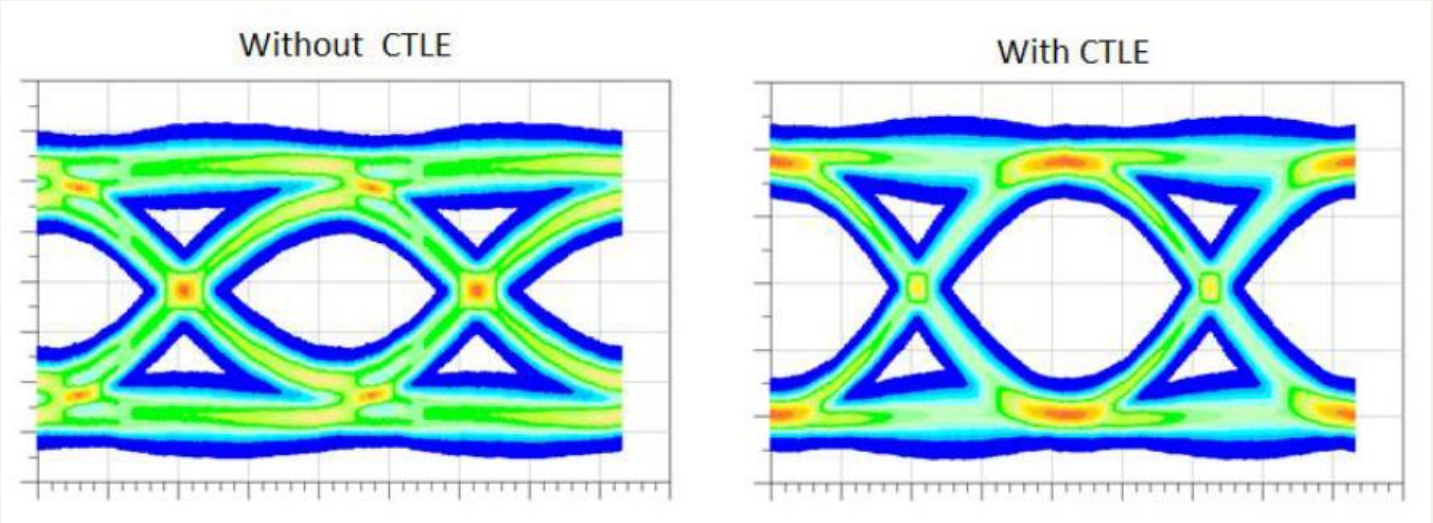
- CTLE fp1 Vs. Gain_dc sensitivity sweep at 6 GHz bandwidth
  - BER 10^{-16} eye width not very sensitive to fp2 around 5GHz
  - BER 10^{-16} eye width increase with higher Gain_dc



BER 10-16 eye width from fp1 and gain_dc at 6GHz bandwidth (fp2)

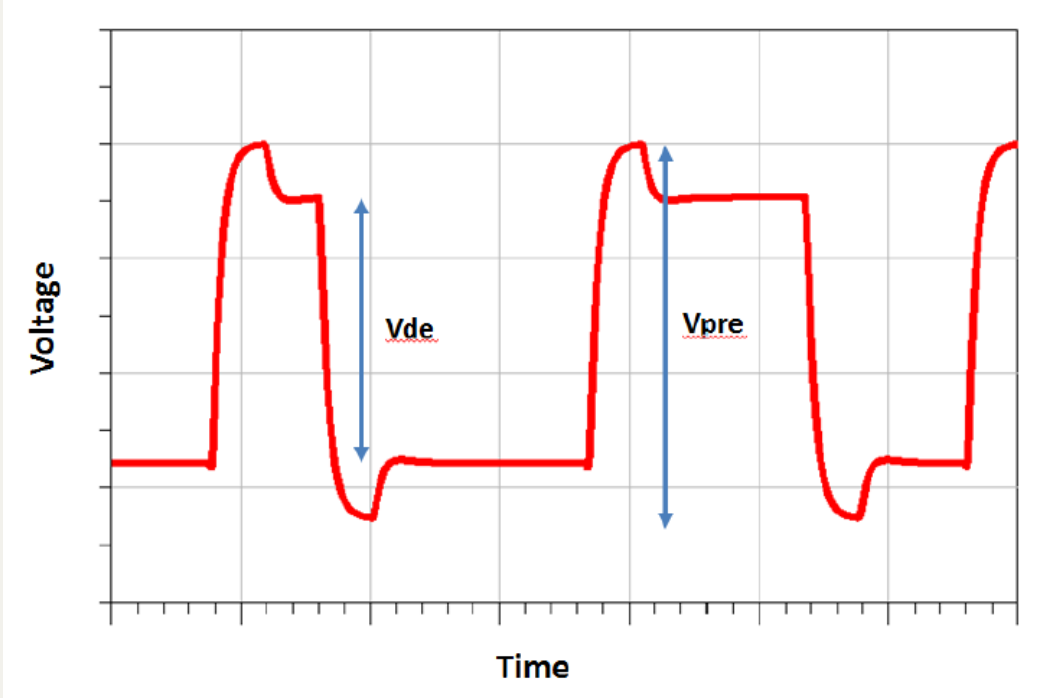
CTLE Optimization -- 2400Mbps DDR4

- significant BER 10^{-16} eye width opening is achieved with optimized CTLE



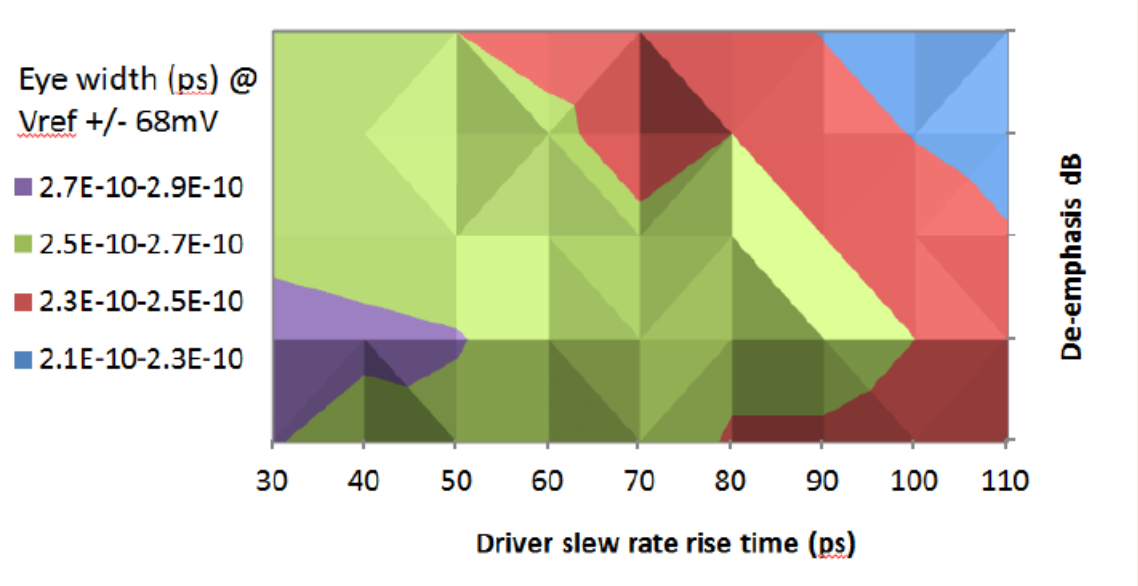
De-emphasis Optimization

- De-emphasis dB level is defined as 20*log(Vde/Vpre)



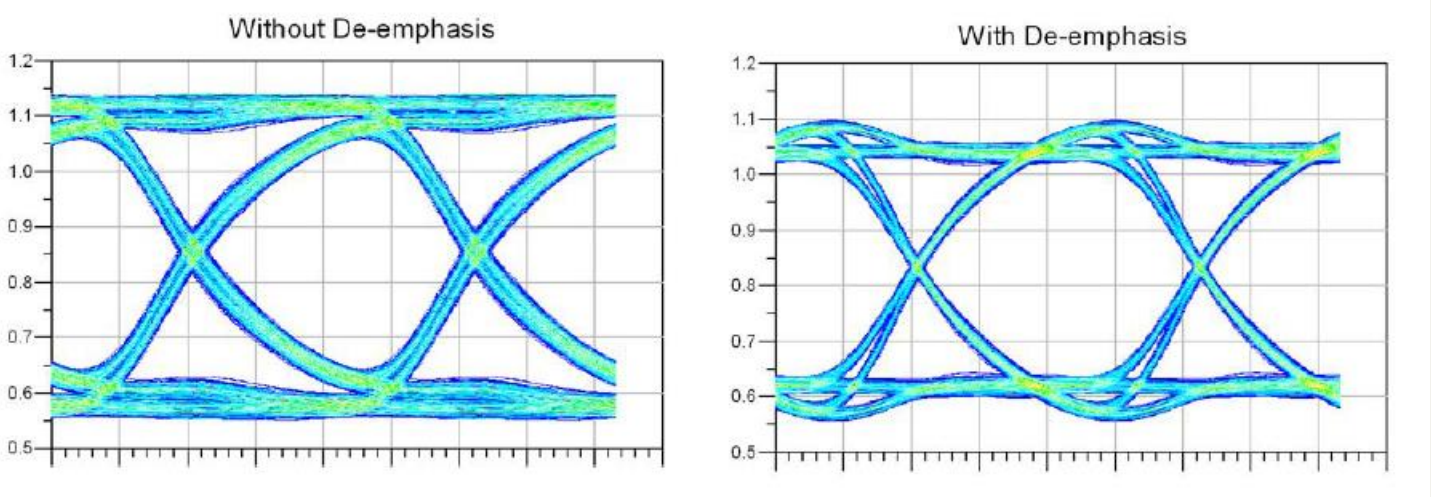
De-emphasis Optimization

- Optimal De-emphasis dB can be identified for driver slew rate



De-emphasis Optimization – 2400Mbps DDR4

- 10-20ps BER 10^{-16} eye width opening achieved with optimized dB setting



Summary

- A statistical simulation engine is introduced for designing DDR4 system to JEDEC 10-16 BER target
- Effects of driver de-emphasis and Rx CTLE on DDR4 timing at BER target of 10-16 are investigated
- De-emphasis and CTLE are effective techniques to mitigate jitter and achieve DDR4 design target after optimization.