DesignCon® 2014

13-TU1, Tuesday Jan 28th, 1st Speaker 9:00 am to 9:20

28 Gb/s SERDES Channel Overview

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XILINX ALL PROGRAMMABLE.

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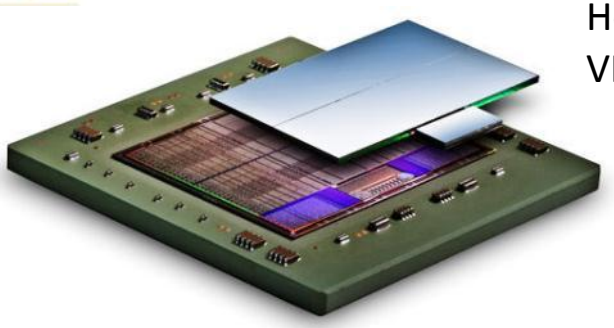
UBM Tech

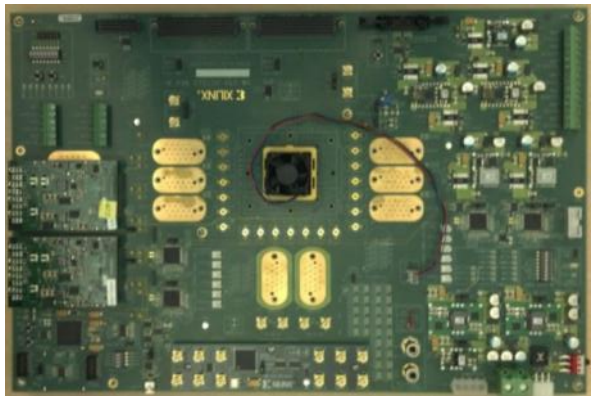
Introduction

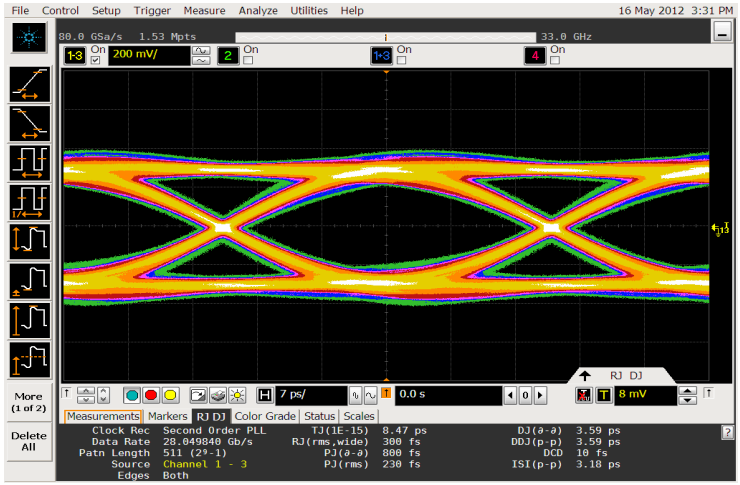
- SerDes links running at 28Gb/s
- Understanding performance at device pin is important
- Need to characterize the transmitter at device pin
- Measurement is dependent on Channel Fixture
  - PCB Channel
  - Connectors
  - Cables
- Channel Fixture de-embedding required to observe launch waveform

28nm FPGA with GTZ XCVR 7H580T

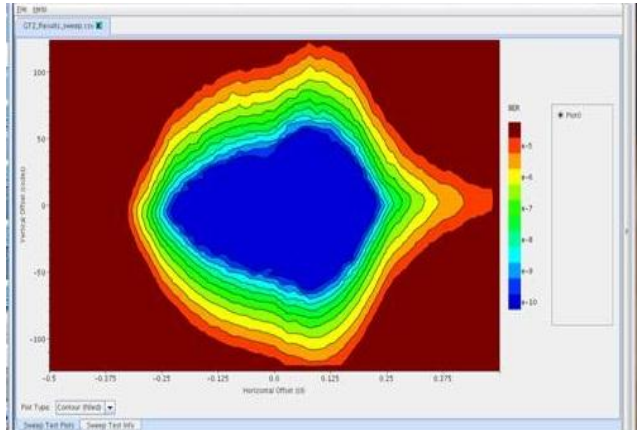


Heterogeneous
VH580T



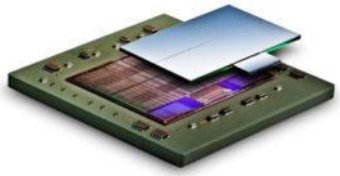


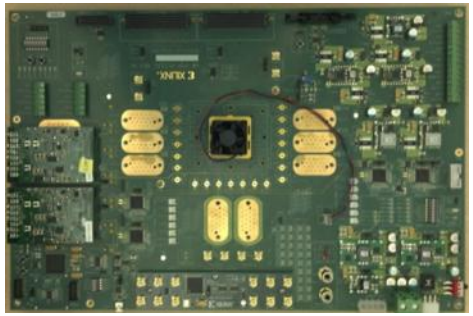
VH580T GTZ TX
Eye Diagram: 28.05Gb/s

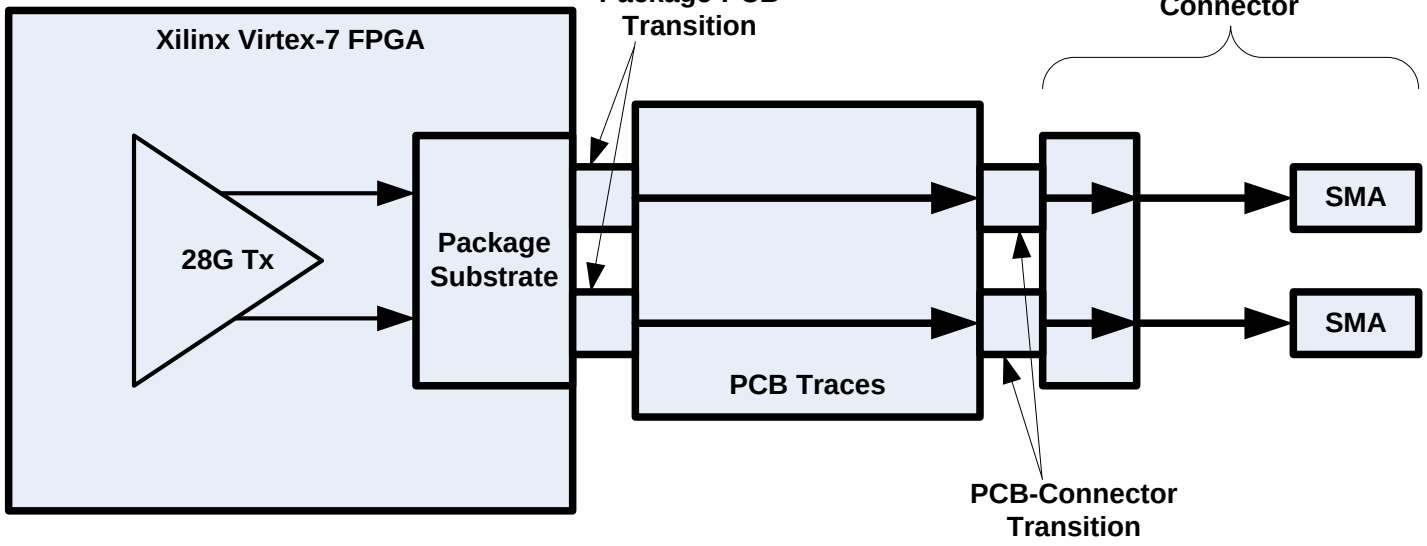


VH580T GTZ
RX Eye Scan: 28.05Gb/s:
Thru 12.5dB Trace

28G Fixture Channel

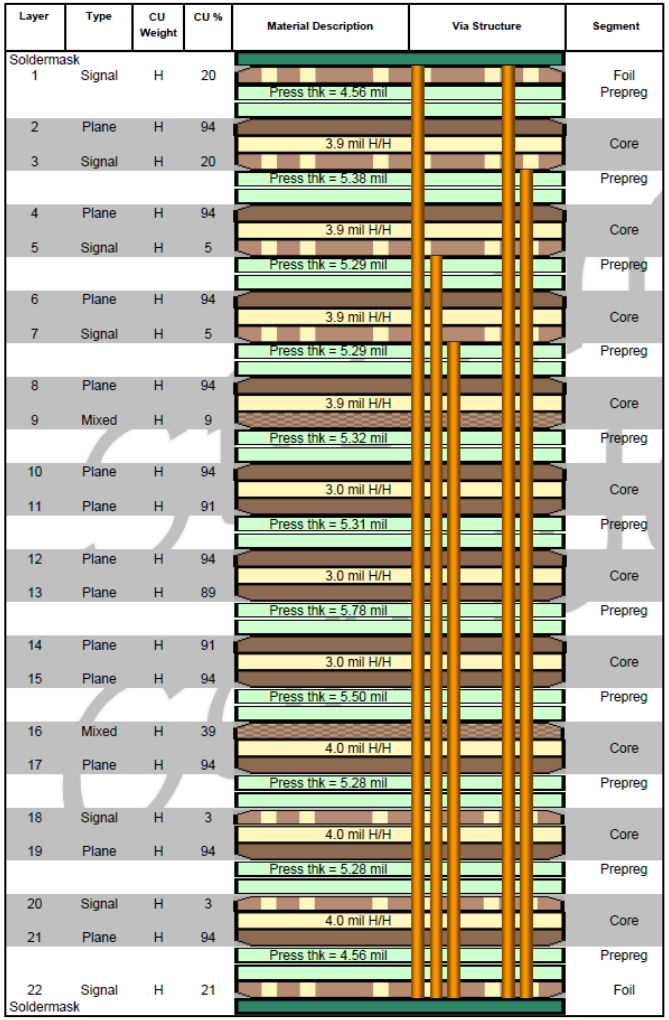






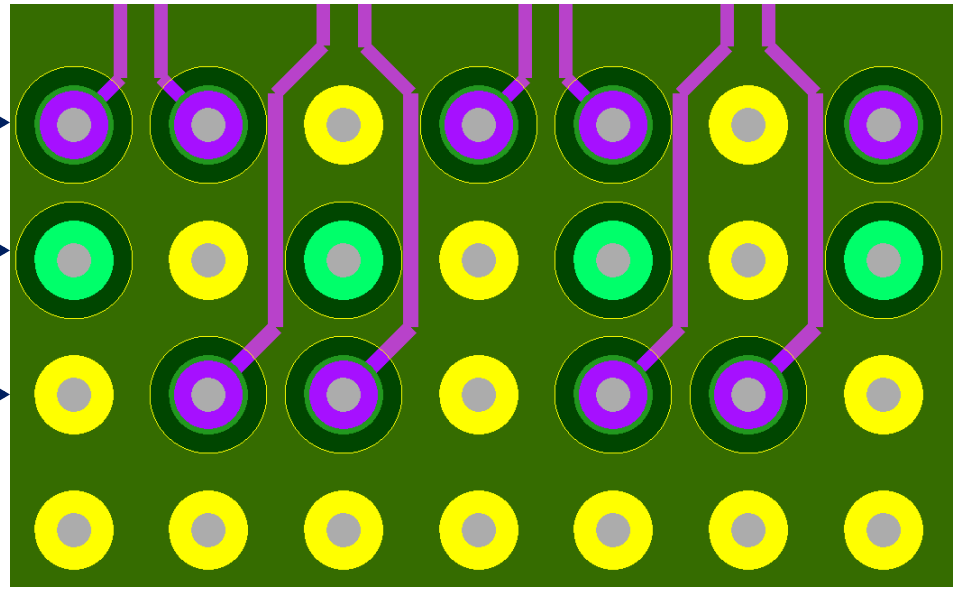
Physical Description PCB Stackup

- 22 Layers
- HS signal layers: Panasonic Megtron6
- Other layers: ISOLA 370HR - FR4
- For Megtron6 and 370HR interleaved in lower layers for mechanical stability
- For economic reasons other layers are standard FR4 (ISOLA 370HR)



Physical Description Pin/Via Breakout

- Highspeed Signal Pin pad (Backdrilled)
- Standard Signal Pin pad (not Backdrilled)
- Ground Via (Not Backdrilled)

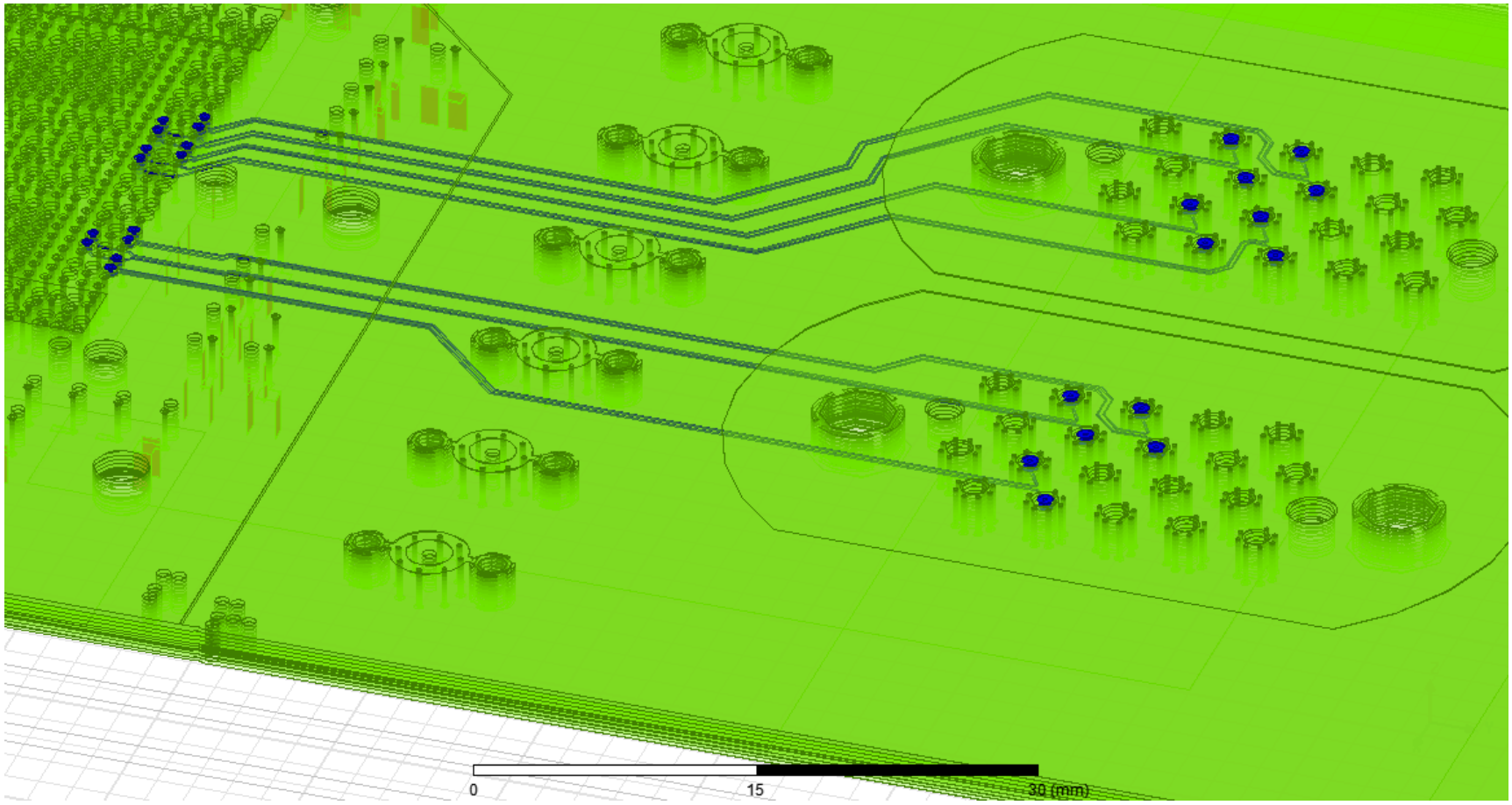


Vias

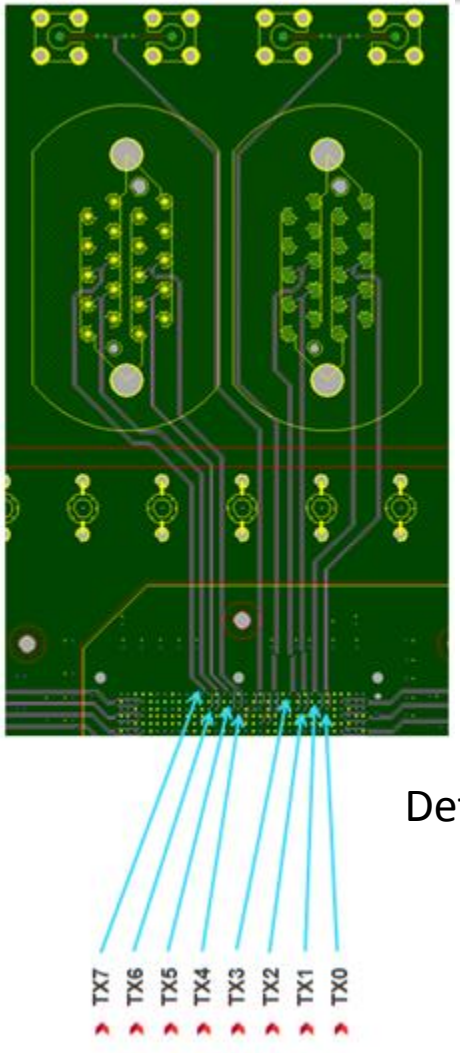
- 10 mil Drill
- 20 mil pad
- 28 mil anti-pad

Backdrill – 8 mils of target layer +/- 3mils

Physical Description PCB Layout

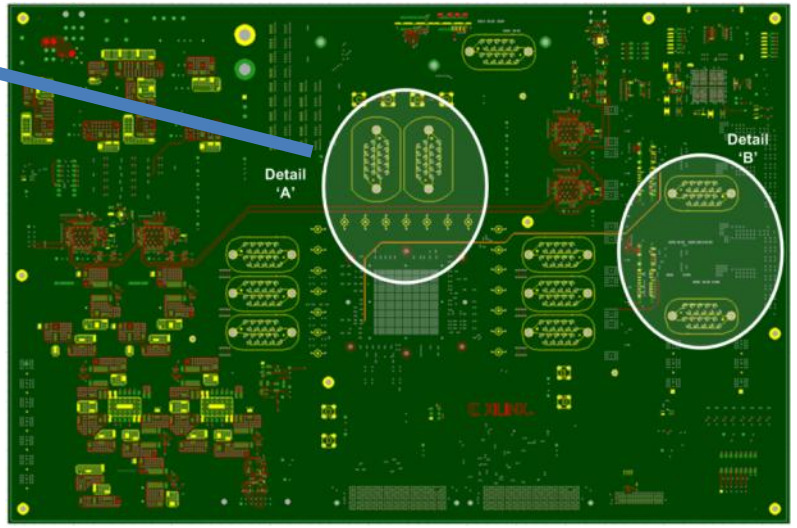


Channel/Physical - PCB

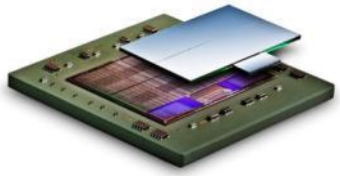


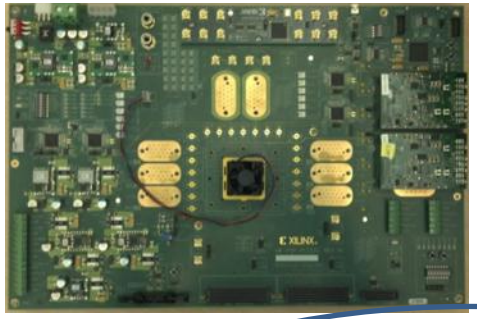
Detail ‘A’

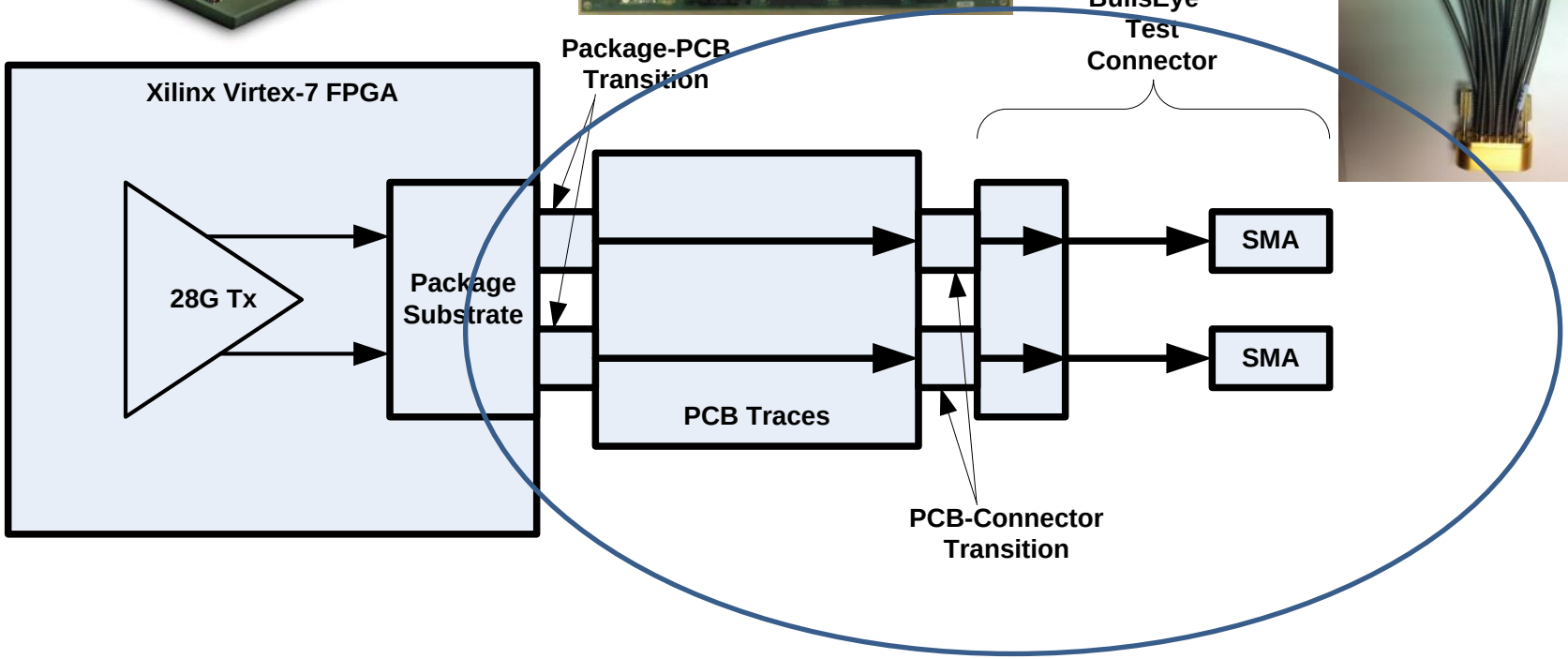
Net	Etch Length (in)	Routing Layer	Trace Width (mil)	Trace Spacing (mil)
TX0	2.683	5	3.75	8.25
TX1	2.293	5	3.75	8.25
TX2	2.298	5	3.75	8.25
TX3	2.501	5	3.75	8.25
TX4	2.698	5	3.75	8.25
TX5	2.373	5	3.75	8.25
TX6	2.607	5	3.75	8.25
TX7	2.804	5	3.75	8.25



Fixture De-Embed Challenge







Next Speaker

- 28 Gb/s SERDES Channel Overview – Romi Mayder and Jack Carrel (20min)
- Fixture S-parameter model from 2x Fixture Physical Test Structures – Mike Resso (35 min)
- Fixture S-parameter model from Simulated Measurement Based Model – Heidi Barnes (35 min)
- Waveform Measurements at the DUT using S-parameter model de-embedding. Rob Sleigh (1 hour)
- Lessons Learned – Jack Carrel (15 min)